

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 32

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JEFFREY M. ABRAMSON,
HATHAM AKKARY,
ANDREW F. GLEW,
GLENN J. HINTON,
KRIS G. KONIGSFELD,
and
PAUL D. MADLAND

Appeal No. 1999-2398
Application No. 08/825,427

ON BRIEF

Before HAIRSTON, BARRETT, and DIXON, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 5, 7 through 11, 13 through 28, 30 through 34, 36 through 46 and 48 through 68. After submission of the brief (paper number 27), the examiner indicated (answer, page 25)

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that claims 53 through 55 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and that claims 56 through 58, 67 and 68 are allowed. Accordingly, claims 1 through 5, 7 through 11, 13 through 28, 30 through 34, 36 through 46, 48 through 52 and 59 through 66 remain before us on appeal.

The disclosed invention relates to a processor for executing at least one store instruction in a computer system.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A method for performing a store operation in a computer system comprising the steps of:

creating a first operation and a second operation in response to the store operation, wherein the first operation includes an address calculation for the store operation and the second operation includes a data calculation for the store operation;

executing the first operation and the second operation as individual instruction entities, wherein the time during which the first operation is executed is independent of the time during which the second operation is executed; and

recombining the first operation and the second

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operation, wherein an address generated by executing the first operation and data produced by executing the second operation are combined for dispatch to memory as a single operation.

The references relied on by the examiner are:

Matsuo et al. (Matsuo)	5,313,644	May 17, 1994	
			(filed Nov. 28, 1990)
Popescu et al. (Popescu)	5,487,156	Jan. 23, 1996	
			(filed Dec. 5, 1990)

Claims 1 through 5, 7 through 11, 13 through 28, 30 through 34, 36 through 46, 48 through 52 and 59 through 66 stand rejected under 35 U.S.C. § 103 as being unpatentable over Matsuo in view of Popescu.

Reference is made to the briefs (paper numbers 27 and 29) and the answer (paper number 28) for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the obviousness rejection of the claims on appeal.

The examiner acknowledges (answer, page 4) that "Matsuo

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does not explicitly teach creating separately address and data calculations in response to store operations," but adds that Matsuo discloses (Figure 26; column 12, lines 22 through 35) address calculations performed by address calculation unit 24, and data operations independently performed by data operation unit 26 in response to general instructions. According to the examiner (answer, page 4), general instructions "inherently include store operations." The examiner also acknowledges (answer, page 5) that Matsuo does not explicitly teach recombining the calculated address and data for dispatch to memory as a single operation. For such a teaching of address and data recombination before storage in memory, the examiner turns to Popescu, and concludes that "[i]t would have been obvious to one of ordinary skill in the art at the time of the invention to modify Matsuo in light of Popescu by combining the results of address and data calculations for storage to memory."

Instead of challenging the proposed combination of reference teachings, appellants have chosen to challenge the examiner's contentions concerning the sole teachings of Matsuo

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(brief, page 8). Appellants argue (brief, pages 5 and 6)
that:

Matsuo discloses an instruction decoding unit coupled to an address calculation unit and a data operation unit. See Fig. 26. However, Appellants respectfully submit that simply disclosing a single instruction unit coupled to multiple functional units does not teach or suggest creating multiple instruction entities based on an original instruction where the multiple instruction entities are executed independent of each other. Multiple functional units with a single instruction unit is [sic, are] known for use with pipelined architectures. The stages of the pipeline are performed in a specific order for each instruction.

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This theoretically allows instructions to be independent of each other, but does not suggest different portions of a single instruction can be executed independent of each other as claimed.

While *Matsuo* discloses both an address calculation unit and a data operation unit, operations performed by the two units for a single store instruction are not independent of each other with respect to a single instruction. Further, *Matsuo* does not teach or suggest creating a first operation and a second operation in response to a store (or any other type of) instruction. *Matsuo* cannot teach or suggest independent execution of operations based on a single store operation because *Matsuo* teaches pipelined execution of each instruction without decomposition of each instruction.

We agree with appellants' arguments. Thus, the obviousness rejection of claims 1¹ through 5, 7 through 11, 13

¹ It appears that the broad limitations of claim 1, and other claims on appeal, read on the admitted prior art (specification, pages 1 and 2). For example, "[i]n the prior art, a store operation included an address calculation and a data calculation," and "[t]hese two calculations are performed by different hardware in the computer system and require different resources." The admitted prior art goes on to explain that "the store operation is performed in response to one instruction, or one part of an instruction, wherein the data calculation is performed first and, once complete, the address calculation occurs" In other words, "the time during which the first operation is executed is independent of the time during which the second operation is executed" as claimed. Thereafter, the calculated address and the data are recombined and dispatched to memory as a single operation.

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through 28, 30 through 34, 36 through 46, 48 through 52 and 59
through 66 is

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reversed because the applied references neither teach nor would have suggested the specifically claimed execution of a store operation.

DECISION

The decision of the examiner rejecting claims 1 through 5, 7 through 11, 13 through 28, 30 through 34, 36 through 46, 48 through 52 and 59 through 66 is reversed.

REVERSED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
)	
)	
)	
LEE E. BARRETT)	BOARD OF PATENT
Administrative Patent Judge)	APPEALS AND
)	INTERFERENCES
)	
)	
JOSEPH L. DIXON)	
Administrative Patent Judge)	

KWH:hh

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BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN
12400 WILSHIRE BLVD., SEVENTH FLOOR
LOS ANGELES, CA 90025