

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte THANG M. TRAN

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Appeal No. 1999-1888  
Application No. 08/473,504

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ON BRIEF

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Before HAIRSTON, BARRETT, and GROSS, Administrative Patent Judges.  
GROSS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1 through 14 and 16 through 26. Claim 15 has been canceled. On page 17 of the Examiner's Answer, the examiner indicates that claim 4 is objected to as being dependent upon a rejected base claim. Accordingly, claims 1 through 3, 5 through 14, and 16 through 26 remain before us on appeal.

Appellant's invention relates to a data address prediction structure for a superscalar microprocessor. The processor fetches data associated with a data prediction address into a data buffer and accesses the data buffer during a decode stage of an instruction processing pipeline. Thus, an implicit memory

Appeal No. 1999-1888  
Application No. 08/473,504

read operation associated with an instruction is performed prior to the instruction arriving at the functional unit which forms the execute stage of the instruction processing pipeline, thereby reducing the number of clock cycles required by the functional unit. Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A method for predicting a data address which will be referenced by a plurality of instructions residing in a basic block when said basic block is fetched, comprising:

generating a data prediction address;

fetching data associated with said data prediction address from a data cache into a data buffer; and

accessing said data buffer for load data from a decode stage of an instruction processing pipeline.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Eickemeyer (Eickemeyer I)	5,313,634	May 17, 1994
Eickemeyer et al. (Eickemeyer II)	5,377,336	Dec. 27, 1994
Kusano	5,412,786	May 02, 1995

Claims 1 through 3 stand rejected under 35 U.S.C. § 103 as being unpatentable over Eickemeyer II.

Claims 5 through 14 and 16 stand rejected under 35 U.S.C. § 103 as being unpatentable over Eickemeyer II in view of Eickemeyer I.

Claims 17 through 25 stand rejected under 35 U.S.C. § 103 as being unpatentable over Eickemeyer I in view of Eickemeyer II.

Appeal No. 1999-1888  
Application No. 08/473,504

Claim 26 stands rejected under 35 U.S.C. § 103 as being unpatentable over Eickemeyer I in view of Kusano.

Reference is made to the Examiner's Answer (Paper No. 16, mailed February 1, 1999) for the examiner's complete reasoning in support of the rejections, and to appellant's Brief (Paper No. 15, filed November 16, 1998) and Reply Brief (Paper No. 17, filed April 5, 1999) for appellant's arguments thereagainst.

#### OPINION

We have carefully considered the claims, the applied prior art references, and the respective positions articulated by appellant and the examiner. As a consequence of our review, we will reverse the obviousness rejections of claims 1 through 3, 5 through 14, and 16 through 26.

Independent claim 1 recites accessing a data buffer "from a decode stage of an instruction processing pipeline." The examiner admits (Answer, page 4) that Eickemeyer II fails to "explicitly state" this claimed limitation, but asserts that it would have been obvious "since Eickemeyer shows that the load data is available in the decode stage," and "because doing so would have eliminated the normal data fetch cycle from the execution unit pipeline."

Appellant (Brief, pages 5-6) explains that Figure 2 of Eickemeyer II shows that the decode unit accesses history buffer

Appeal No. 1999-1888  
Application No. 08/473,504

201, but not a data buffer. The examiner, rather than responding to appellant's argument, merely repeats the rejection verbatim. We fail to see where Eickemeyer II shows the load data being available in the decode stage. Instead, Figure 2 clearly indicates that the accessing of load data occurs after the decode stage. Accordingly, we cannot sustain the rejection of claims 1 through 3.

As to claims 5 through 14 and 16, the examiner adds Eickemeyer I, which also shows (in Figure 2) accessing of load data occurring after the decode stage. Consequently, as Eickemeyer I fails to cure the deficiency of Eickemeyer II, we will not sustain the rejection of claims 5 through 14 and 16.

Independent claim 17 recites that the decode stage is "configured to access said data buffer." The examiner relies on Eickemeyer I and II. Appellant argues (Brief, page 10), and as stated above, the two references show accessing of the load data occurring after the decode stage, not during the decode stage. Again the examiner responds to appellant's argument by repeating the rejection verbatim. Therefore, we cannot sustain the rejection of claims 17 through 25.

Lastly, regarding claim 26, the examiner admits (Answer, page 16) that Eickemeyer I "does not explicitly show the claimed limitation of fetching data associated with said plurality of

Appeal No. 1999-1888  
Application No. 08/473,504

said instructions from said data prediction address in a data cache; and placing said data associated with basic block of instructions into a data buffer." The examiner turns to Kusano to supply the limitations lacking from Eickemeyer I.

Appellant contends (Brief, page 11) that "Kusano predicts and prefetches a single data address based upon a previous data address." Appellant thus concludes that neither reference discloses a basic block of instructions and fetching data associated with the plurality of instructions in the basic block. We find no disclosure in either reference of a block of instructions. Therefore, we agree with appellant. Furthermore, the examiner has once again repeated the rejection in lieu of responding to appellant's argument. Thus, the examiner has not persuaded us of any error in appellant's argument. Accordingly, we will not sustain the rejection of claim 26.

Appeal No. 1999-1888  
Application No. 08/473,504

CONCLUSION

The decision of the examiner rejecting claims 1 through 3, 5 through 14, and 16 through 26 under 35 U.S.C. § 103 is reversed.

REVERSED

KENNETH W. HAIRSTON	)	
Administrative Patent Judge	)	
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	)	
	)	BOARD OF PATENT
LEE E. BARRETT	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
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ANITA PELLMAN GROSS	)	
Administrative Patent Judge	)	

Appeal No. 1999-1888  
Application No. 08/473,504

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