

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte TAKUMI HASEGAWA

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Appeal No. 1999-1797  
Application No. 08/635,197

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HEARD: MAY 10, 2001

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Before KRASS, BARRETT, and BLANKENSHIP, Administrative Patent Judges.

BLANKENSHIP, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-13, which are all the claims in the application.

We reverse.

### BACKGROUND

The disclosed invention is directed to a system for verifying delays in a logic circuit, using information both prior and subsequent to layout of the circuit. Claim 1 is reproduced below.

1. A delay verification device for performing delay verification for a logic circuit having circuit elements, comprising:

    circuit information storing means for storing circuit information on said logic circuit;

    first delay information storing means for storing first delay information on a delay time between said circuit elements predicted before layout designing of said logic circuit;

    second delay information storing means for storing second delay information on a delay time between said circuit elements computed after layout designing of said logic circuit;

    difference extracting means for comparing said first delay information and said second delay information, and for extracting difference information on a portion of said logic circuit whose delay time of said second delay information is longer than that of said first delay information;

    extracted circuit information obtaining means for searching paths of said logic circuit based on said circuit information and said difference information, extracting a path including said portion of said logic circuit, and storing the extracted path as extracted circuit information; and

    delay analyzing means for analyzing delays of said extracted path using said extracted circuit information.

The examiner relies on the following reference:

Ramachandran et al. (Ramachandran), Combined Topological and Functionality-Based Delay Estimation Using a Layout-Driven Approach for High-Level Applications, IEEE

Appeal No. 1999-1797  
Application No. 08/635,197

Trans. Computer-Aided Design of Integrated Circuits and Systems, vol. 13, no. 12, pp. 1450-60 (Dec. 1994).

Claims 1-13 stand rejected under 35 U.S.C. § 103 as being unpatentable over Ramachandran.

We refer to the Final Rejection (Paper No. 7) and the Examiner's Answer (Paper No. 14) for a statement of the examiner's position and to the Brief (Paper No. 13) and the Reply Brief (Paper No. 15) for appellant's position with respect to the claims which stand rejected.

#### OPINION

The rejection of claim 1 as being obvious in view of Ramachandran is set forth on pages 3 through 7 of the Answer. Appellant contends, as articulated on pages 5 through 10 of the Brief, that the article fails to disclose or suggest the claimed functions performed by the "difference extracting means" and the "extracted circuit information obtaining means."

The rejection, at page 5 of the Answer, points to the right column of page 1458 of Ramachandran as disclosing a type of "extraction." The relevant passage in Ramachandran uses the phrase "extracting the difference." However, we agree with appellant, as advanced on page 7 of the Brief, that the passage misses the mark with respect to the "difference extracting means" requirements of claim 1. The examiner's

Appeal No. 1999-1797  
Application No. 08/635,197

rationale on pages 6 and 7 of the Answer purports to explain why the limitations of claim 1 are rendered obvious by the teachings of the prior art article. Again, however, we are in substantial agreement with appellant's position, as stated in the Reply Brief, that the rejection appears to advance in the wrong direction. Instead of showing how the teachings of Ramachandran would have led the artisan to the subject matter of instant claim 1, the rejection appears to use the teachings to show that the artisan would have recognized the advantages of a system such as that presently claimed.

The reference, at pages 1458 and 1459, describes use of software to study the variations of circuit delay with respect to various possible layout configurations. The phrase "extracting the difference" refers to finding the difference between two paths, with a "100% difference" representing completely different critical paths. In our view the reference fails to teach or suggest the specific requirements of claim 1.

The allocation of burdens requires that the USPTO produce the factual basis for its rejection of an application under 35 U.S.C. § § 102 and 103. In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984) (citing In re Warner, 379 F.2d 1011, 1016, 154 USPQ 173, 177 (CCPA 1967)). The one who bears the initial burden of presenting a prima facie case of unpatentability is the examiner. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). Since the examiner has not convincingly explained where the suggestion for the proposed modification of Ramachandran lies, and we do not find any suggestion for the modification in the evidence

Appeal No. 1999-1797  
Application No. 08/635,197

before us, the rejection appears to be based on a hindsight reconstruction of appellant's invention.

Appellant, on pages 12 and 13 of the Brief, refers to limitations in independent claims 8 and 12 which are argued as rendering the subject matter as a whole nonobvious over the reference. We agree that at least the fourth and fifth steps in claim 8 and claim 12, respectively, are not disclosed or suggested by Ramachandran. Since a prima facie case of obviousness has not been established for any of the independent claims on appeal, we do not sustain the rejection of claims 1-13.

#### CONCLUSION

The rejection of claims 1-13 is reversed.

Appeal No. 1999-1797  
Application No. 08/635,197

REVERSED

ERROL A. KRASS	)	
Administrative Patent Judge	)	
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	)	BOARD OF PATENT
LEE E. BARRETT	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
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HOWARD B. BLANKENSHIP	)	
Administrative Patent Judge	)	

Appeal No. 1999-1797  
Application No. 08/635,197

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