

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 11

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SUDHIR MADAN

Appeal No. 1999-1631
Application 08/733,586¹

ON BRIEF

Before MARTIN, GROSS, and DIXON, Administrative Patent Judges.

MARTIN, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1, 2, and 4-15, all of the pending claims, under 35 U.S.C. §§ 112 and 102.

We affirm-in-part and reverse-in-part.

A. The invention

¹ Application for patent filed October 18, 1996.

The invention relates to the layout design of static random access memory (SRAM) cells. Figure 1A is the circuit diagram of

a prior art SRAM having: a first inverter 12, which includes a p-type pull-up transistor 20 and an n-type pull-down transistor 24; a second inverter 14, which includes a p-type pull-up transistor 22 and an n-type pull-down transistor 26; and two pass transistors, 16 and 18. In the prior art layout shown in Figure 1B, gates 90 and 94 of transistors 20 and 24 in inverter 12 are offset in the vertical (i.e., y) direction but not in the horizontal direction. The same relationship applies to gates 92 and 96 of transistors 22 and 26 in inverter 14.

In the prior art layout of Figure 1C, gate 90 of transistor 20 is offset horizontally to the left relative to gate 94 of transistor 24, while gate 92 of transistor 22 is offset horizontally to the right relative to gate 96 of transistor 26.

In appellant's first embodiment (Figure 2), both horizontal offsets are in the same direction, i.e., gate 140

of transistor 106 (in inverter 102) is offset horizontally to the right relative to gate 142 of transistor 110 (in inverter 102), and gate 144 of transistor 108 (in inverter 104) is offset horizontally to the right relative to gate 146 of transistor 112 (in inverter 104).

In appellant's second embodiment (Figure 3), the horizontal offsets are in the same direction but in different amounts, i.e., gate 240 of transistor 206 (inverter 202) is offset horizontally to the right by a first amount relative to gate 242 of transistor 210 (inverter 202), and gate 244 of transistor 208 (inverter 204) is offset horizontally to the right by a second, smaller amount relative to gate 246 of transistor 212 (inverter 204).

The amount of horizontal offset in appellant's embodiments can be described as the difference between the p-channel mean (x_{pm}) and the n-channel mean (x_{nm}), where the x co-ordinates of the center points of the gates of the first and second p-channel transistors are x_{p1} and x_{p2} , the x co-ordinates of the center points of the gates of the first and second n-channel transistors are x_{n1} and x_{n2} , the p-channel mean (x_{pm}) equals $(x_{p1}+x_{p2})/2$, and the n-channel mean (x_{nm})

equals $(x_{n1}+x_{n2})/2$ (Specification at 6, ll. 19-26). The difference between the two means can be in the range from the minimum feature size of a given technology (e.g., 0.5 microns) up to one-half the width of the cell (id. at 6, l. 26 to p. 7, l. 1).

B. The claims

The independent claims, i.e., claims 1, 5, and 10, read as follows:²

1. A static random access memory (SRAM) cell comprising:

a pair of cross-coupled inverters, a first of said inverters comprising a first p-channel pull-up transistor and a first n-channel pull-down transistor, a second of said inverters comprising a second p-channel pull-up transistor and a second n-channel pull-down transistor, wherein a gate of said first p-channel pull-up transistor is offset from a gate of the first n-channel pull-down transistor in the same horizontal direction as a gate of the second p-channel pull-up transistor is offset from a gate of the second n-channel pull-down transistor, and said n-channel pull-down transistors are laterally aligned;

a pair of bitlines extending in a vertical direction; and

² In Claim 10 as reproduced in the Appendix to the Brief, line 2 incorrectly includes the term "gate" after "transistor" (first occurrence). The examiner also correctly notes (Answer at 3) that dependent claim 6 is incorrectly reproduced in that Appendix -- the value "0.25" should read "0.5."

a pair of pass transistors connected between said pair of bitlines and said pair of cross-coupled inverters.

5. A static random access memory (SRAM) device comprising a plurality of cells, each of said cells comprising:

a first inverter comprising a first p-channel transistor centered at a first x-co-ordinate [sic; x co-ordinate] and a first n-channel transistor centered at a second x co-ordinate;

a second inverter cross-coupled with said first inverter and comprising a second p-channel transistor centered at a third x co-ordinate and a second n-channel transistor centered at a fourth x-co-ordinate [sic], wherein a mean of said first and third x co-ordinates is unequal to a mean of said second and fourth x co-ordinates, said first and second n-channel transistors being roughly aligned which defines the x direction; and

a pair of pass transistors connected to said first and second inverters.

10. A static random access memory (SRAM) cell comprising:

a first inverter comprising a first p-channel transistor and a first n-channel transistor, said first p-channel transistor being offset in both the horizontal and vertical directions from said first n-channel transistor;

a second inverter cross-coupled with said first inverter and comprising a second p-channel transistor and a second n-channel transistor, said second p-channel transistor being offset from the second n-channel transistor in the same horizontal and vertical directions as the first p-channel and first n-channel transistors, and with said first and

second n-channel transistors horizontally aligned.

C. The reference and rejections

The examiner relies on the following U.S. patent:

Harari	4,132,904	Jan. 2,
1979		

Claim 6 stands rejected under 35 U.S.C. § 112, ¶ 1 for lacking written description support in the disclosure as filed and for being based on a nonenabling disclosure.

Claims 2, 6, 7, and 14 stand rejected under § 112, ¶ 2 for indefiniteness.

Claims 1, 2, and 4-15 stand rejected under § 102 as anticipated by Harari.

D. Appellant's burden of persuasion

Anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. In re King, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986). Thus, appellant's burden on appeal with respect to a rejection for anticipation is to identify at least one claimed element that the examiner has failed to show is disclosed or inherent in the reference. See Gechter v.

Davidson, 116 F.3d 1454, 1460, 43 USPQ2d 1030, 1035 (Fed. Cir. 1997) ("[W]e expect that the Board's anticipation analysis be conducted on a limitation by limitation basis, with specific fact findings for each contested limitation and satisfactory explanations for such findings [footnote omitted]."). Compare In re Rouffet, 149 F.3d 1350, 1355 47 USPQ2d 1453, 1455 (Fed. Cir. 1998), which explains that "[o]n appeal to the Board, an applicant can overcome a [35 U.S.C. § 103] rejection by showing insufficient evidence of prima facie obviousness or by rebutting the prima facie case with evidence of secondary indicia of nonobviousness."

E. The § 112, ¶ 1 rejection of claim 6

Dependent claim 6, which stands rejected under § 112, ¶ 1, reads as follows:

6. The SRAM device of claim 5, wherein a difference between the mean of said first and third x co-ordinates and the mean of said second and fourth x co-ordinates is in the range of 0.5 microns to one half of a width of said SRAM cell.

The examiner's contention that this claim lacks written description support in the specification is incorrect; this claim language has clear written description support in the following sentence, which bridges pages 6 and 7 of the

specification: "A difference between the p-channel mean x_{pm} and the n-channel mean x_{nm} may be in the range of the minimum feature size of a given technology (e.g., 0.5 microns) to one half of the cell width."

The examiner's contention that this claim lacks an enabling disclosure is unconvincing because it is based on insufficient reasoning. In re

Marzocchi, 439 F.2d 220, 223-24, 169 USPQ 367, 369-70 (CCPA 1971) explains:

As a matter of Patent Office practice, then, a specification disclosure which contains a teaching of the manner and process of making and using the invention in terms which correspond in scope to those used in describing and defining the subject matter sought to be patented must be taken as in compliance with the enabling requirement of the first paragraph of § 112 unless there is reason to doubt the objective truth of the statements contained therein which must be relied on for enabling support. Assuming that sufficient reason for such doubt does exist, a rejection for failure to teach how to make and/or use will be proper on that basis; such a rejection can be overcome by suitable proofs indicating that the teaching contained in the specification is truly enabling.

. . . it is incumbent upon the Patent Office, whenever a rejection on this basis is made, to explain why it doubts the truth or accuracy of any statement in a supporting disclosure and to back up assertions of its own with acceptable evidence or reasoning which is inconsistent with the contested statement. Otherwise, there would be no need for the applicant to go to the trouble and expense of supporting his presumptively accurate disclosure. Cf. In re Gazave, 379 F.2d 973, 54 CCPA 1524[, 154

USPQ 92] (1967); In re Chilowsky, 229 F.2d 457,
43 CCPA 775[, 108 USPQ 321] (1956).

Accord In re Wright, 999 F.2d 1557, 1563, 27 USPQ2d 1510, 1513
(Fed. Cir. 1993). Although, as the examiner correctly notes
(Answer at 3), the embodiment depicted in Figure 3 has a mean
difference of value 1.55 microns (Specification at 9, l. 17),
which is also the mean difference value the embodiment
depicted in Figure 2 (id. at 7, l. 3), the absence of an
embodiment having a mean difference of about 0.5 microns is
insufficient in and of itself to satisfy the examiner's
initial burden to show nonenablement. Note that in Wright,
which involved an application that disclosed a single working
example within the scope of the claim, the court held that the
examiner and the Board had given adequate reasons why one
skilled in the art would have been unable to make other
embodiments within the scope of the claim. 999 F.2d at 1560-
64, 27 USPQ2d at 1511-15. See also In re Strahilevitz, 668
F.2d 1229, 1232, 212 USPQ 561, 563 (CCPA 1982):

We recognize that working examples are desirable in
complex technologies and that detailed examples can
satisfy the statutory enablement requirement.
Indeed, the inclusion of such examples here might
well have avoided a lengthy and, no doubt, expensive
appeal. Nevertheless, as acknowledged by the board,
examples are not required to satisfy section 112,

first paragraph. See, e.g., In re Stephens, 529 F.2d 1343, 188 USPQ 659 (CCPA 1976); In re Borkowski, 57 CCPA 946, 422 F.2d 904, 164 USPQ 642 (1970); In re Gay, 50 CCPA 725, 309 F.2d 769, 135 USPQ 311 (1962).

For the foregoing reasons, the rejection of claim 6 under § 112, ¶ 1 is reversed.

F. The § 112, ¶ 2 rejection of claims 2, 6, 7, and 14

Claim 2 reads as follows: "The SRAM cell of claim 1 wherein the cell vertical dimension to horizontal dimension ratio is less than 2:1." The same limitation appears in claims 7 and 14. Claim 6 is reproduced above.

The examiner's rejection for indefiniteness reads as follows (Answer at 3):

In claims 2, 7, [and] 14 the cell "vertical dimension" and "horizontal dimension" do not have a clear antecedent basis absent claiming what bounds the "vertical dimension" and "horizontal dimension" of a cell. In claim 6, a "width" of [a] cell is vague absent claiming what bounds the "width" of [a] cell. What comprises the "vertical dimension[,"] "horizontal dimension" and "width" of a cell is not claimed. The scope is thereby indefinite.

As the examiner has not objected to the use of the terms "horizontal" and "vertical" in the other claims, we understand the examiner's position to be that it is not clear how to measure the horizontal dimension (i.e., width) or the vertical

dimension (i.e., length) of a cell. Appellant's argument that cell width is defined in the paragraph bridging pages 1 and 2 of the specification is unconvincing, because that paragraph does not explain how these dimensions are measured. Nor is this measurement technique apparent from appellant's disclosed examples. Referring to Figures 2 and 3, the cell origins (0,0)

(Specification at 7, l. 3; at 9, l. 17) are not aligned with the left-most and bottom-most points of the structure depicted in those figures. Instead, the cell origins appear to be located at the lower left-hand corners of features 180 (Fig. 2) and 280 (Fig. 3), which are described as subsequent metal layers "used to route ground, Vss" (id. at 7, ll. 14-15; at 9, ll. 23-25³).

However, the points which correspond to the upper right-hand corners of the cells are not identified in the figures, thereby leaving it unclear how the width and length of the cell are measured. Furthermore, it is not understood how the cell width in the Figure 2 layout can be only 6.9 microns (id.

³ The second cited passage incorrectly gives the reference numeral in Figure 3 as 180 instead of 280.

at 7, l. 1) when xp2, the center point of gate 144 (id. at 6, ll. 22-24), is 7.0 microns (id. at 7, l. 2).

The rejection of claims 2, 6, 7, and 14 under § 112, ¶ 2 is therefore affirmed.

G. The § 102 rejection of claims 1, 2, and 4-15

In view of our affirmance of the § 112, ¶ 2 rejection of claims 2, 6, 7, and 14, we cannot affirm the § 102 rejection to the extent it is directed to those claims. Cf. In re Steele, 305 F.2d 859, 862-63, 134 USPQ 292, 295 (CCPA 1962) (improper to rely on speculation as to meaning of claim for § 103 purposes).

Consequently, we will consider the merits of the § 102 rejection only as to claims 1, 4, 5, 8-13 and 15.

Although, as appellant correctly notes (Brief at 4), the final Office action failed to identify the paragraph of § 102 on which the rejection is based, the Answer (at 7) indicates it is based on paragraphs (a), (b), and (e).⁴ Also, the manner in which the examiner proposes to read the claims on the reference, which was not explained in the final Office

⁴ Where, as here, the reference constitutes a statutory bar under § 102(b), there is no need to alternatively base the rejection on § 102(a) or (e).

action, is explained in the Answer (at 4-7), to which appellant responded with a Reply Brief.

The examiner relies on Figures 2a and 4 of Harari. Figure 4 is a plan view of the latch circuit depicted in schematic form in Figure 2a (col. 5, ll. 42-44). As is apparent from the schematic, a p-channel transistor Q_1 and an n-channel transistor Q_2 form a first inverter that is cross-coupled to a second inverter formed of a p-channel transistor Q_3 and an n-channel transistor Q_4 .⁵ As is also apparent from the symbols in Figure 2a, the n-channel transistors Q_2 and Q_4 are of the floating gate type. Figure 4 includes dashed rectangles surrounding each of the symbols Q_1 - Q_6 . Dashed rectangles 73 and 75, which surround symbols Q_2 and Q_4 , are described as representing the floating gates of those transistors (col. 15, l. 17), as is also apparent from Figure

⁵ Appellant does not deny that the p-channel and n-channel transistors are pull-up and pull-down transistors, respectively, as required by claim 1.

4b, which shows floating gate 75 in cross-section.⁶ That figure also shows a control gate 69a positioned over floating gate 75 (col. 15, ll. 3-9). Because transistors Q_1 and Q_3 do not have floating gates, we assume the unnumbered dashed rectangles surrounding their symbols designate the control gates of those transistors.

The examiner, presumably for the purpose of satisfying claim 1's requirement for "a pair of bit lines extending in a vertical direction," argues that the vertical direction in Harari's Figure 4 is the direction of bit line 61 (Answer at 4), which direction runs left/right in the figure. With the vertical axis thus defined, the horizontal direction in Figure 4 extends along its longer dimension. Appellant's reply brief does not object to the examiner's choice of directions in the reference. Comparing claim 1 to Figure 4 with its directions thus defined, we agree with the examiner that the gate of the first p-channel transistor (Q_1) is offset

⁶ Figure 4b reveals that the channel area is considerably narrower than the floating gate or the control gate. Harari's statement that "[t]he channel area of each transistor is shown by a dashed rectangle which surrounds the symbol (e.g., Q_4) of that transistor in FIG. 4" (col. 14, l. 67 to col. 15, l. 1) therefore should not be understood to mean that the rectangles coincide with the edges of the channel regions.

horizontally to the left of the gate of the first n-channel transistor (Q_2) and that the gate of the second p-channel transistor (Q_3) is offset horizontally to the left of the gate of the second n-channel transistor (Q_4), thereby satisfying claim 1's requirement that these two offsets be in the same horizontal direction. Appellant's argument (Reply Brief at 3) that Harari's discussion of Figures 4 and 4a at column 14, line 48 to column 15, line 25 does not contain "a remote hint of gate offset of any type, let alone the offset as claimed in claim 1" is unpersuasive, as a rejection for anticipation may be based on a feature that is shown in the drawings but not discussed in the specification. See In re van Deventer, 223 F.2d 274, 276, 106 USPQ 121, 123 (CCPA 1955) ("It is quite true that an incidental, or even an accidental, showing may constitute an anticipation and, accordingly, if claim 19 were readable on the drawing of the French patent, it would be immaterial that the taper of the passage is not specifically described.").

Regarding the requirement of claim 1 that the n-channel transistors be "laterally aligned," the examiner argues that transistors Q_2 and Q_4 are laterally aligned because "a line

could be drawn through the gates of Q2, Q4" (Answer at 4). Appellant's reply brief does not address this argument. Nor has appellant explained how the term "laterally aligned" is to be construed and why. Instead, the Brief simply asserts (at 5), without supporting analysis, that "[n]o such feature is taught by Harari." Consequently, appellant has not met his burden of persuasion with respect to this limitation.⁷

Nor does appellant deny that the reference satisfies the remaining limitations of claim 1, i.e., the requirement for a pair of bitlines extending in a vertical direction and a pair of pass transistors connected between the bitlines and the cross-coupled inverters. Consequently, we are affirming the § 102 rejection of claim 1.

Dependent claim 4 specifies that "each gate of each p-channel transistor is offset from the gate of the n-channel transistor in the same inverter by the same distance in the horizontal direction." As appellant has not explained why this limitation is not satisfied when the horizontal direction

⁷ We note in passing that in American Permahedge Inc. v. Barcana Inc., 103 F.3d 1441, 1444, 41 USPQ2d 1614, 1617 (Fed. Cir. 1997), not mentioned by the examiner or appellant, the court held that the ordinary meaning of the term "laterally extending" is to extend sideways irrespective of the angle.

extends in the long dimension of Figure 4, we are also affirming the rejection of this claim.

Appellant's only argument with respect to independent claim 5 is that it is distinguishable from Harari for the reasons given with respect to claim 1 (Reply Brief at 3). In view of our determination that those reasons are unpersuasive as to claim 1, we are also affirming the rejection of claim 5.

Dependent claim 8, which specifies that "the gates of said p-channel pull-up transistors are laterally aligned," is not addressed in the Reply Brief, and the only argument made in the Brief, which is that Harari fails to disclose this feature (Brief at 6), is not based on an explanation of the meaning of the term "laterally aligned." Accordingly, the rejection of this claim is affirmed.

For lack of an argument by appellant, we are also affirming the rejection of dependent claim 9, which specifies that the distances of the two offsets are the same.

Independent claim 10 differs from claims 1 and 5 by specifying that the first and second n-channel transistors are "horizontally aligned." In order to satisfy this limitation, the examiner argues that for purposes of this claim the

horizontal direction is defined by a line connecting the gates of transistors Q_2 and Q_4 . Appellant argues that reading the term "horizontally aligned" on such a line is contrary to the paragraph bridging pages 1 and 2 of the specification. To the extent appellant means that the term "horizontal" must be read as limited to the left-right direction in Harari's Figure 4, we do not agree. However, to the extent appellant is arguing that the "horizontal" direction is limited to one or the other of the orthogonal directions defined by the edges of the features shown in Figure 4, we agree. Because a line connecting the gates of transistors Q_2 and Q_4 would have an angle of about forty-five degrees relative to those orthogonal directions, we hold that those transistors are not horizontally aligned.

Consequently, we are reversing the § 102 rejection of claim 10 and thus of its dependent claims 11-13 and 15.

H. Summary

Summarizing, the § 112, ¶ 1 rejection of claim 6 is reversed; the § 112, ¶ 2 rejection of claims 2, 6, 7, and 14 is affirmed; and the § 102 rejection is affirmed as to claims

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1, 4, 5, 8, and 9 and reversed as to claims 2, 6, 7, and 10-15.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART and REVERSED-IN-PART

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Administrative Patent Judge)	
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