

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SAILESH CHITTIPEDDI

Appeal No. 1999-1576
Application No. 08/347,527

ON BRIEF

Before HAIRSTON, RUGGIERO, and GROSS, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 15 and 18 through 36.

The disclosed invention relates to a semiconductor integrated circuit that has two selectively grown epitaxial layers formed on the top surface of two separate active regions of the integrated circuit. A bipolar transistor is formed on

the first epitaxial layer, and a complementary metal oxide semiconductor device is formed on the second epitaxial layer.

Claim 15 is illustrative of the claimed invention, and it reads as follows:

15. A semiconductor integrated circuit produced by the steps of:

a) forming at least one trench in a silicon substrate to define first and second active device regions on the substrate to be isolated from each other;

b) depositing an electrically insulative material on the substrate to fill the trench with the electrically insulative material, said electrically insulative material having a top surface;

c) planarizing a top surface of the substrate such that the top surface of the substrate in the first and second active device regions is coplanar with the top surface of the electrically insulative material of the filled trench;

d) selectively growing a first epitaxial layer of silicon on top of and in contact with the top surface of the first active device region;

e) selectively growing a second epitaxial layer of silicon on the top surface of the second active device region, the first epitaxial layer and second epitaxial layer being doped with dopant atoms to the same or different dopant concentration, to provide at least two isolated active device regions on the silicon substrate;

f) forming a bipolar transistor on the first epitaxial layer; and

g) forming a complementary metal oxide semiconductor (CMOS) device on the second epitaxial layer.

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The references relied on by the examiner are:

Jastrzebski	4,619,033	Oct. 28, 1986
Eklund	5,049,513	Sept. 17, 1991
Yoneda ¹	62-132342	June 15, 1987

(Japanese patent publication)

Claims 15 and 18 through 36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoneda in view of Eklund and Jastrzebski.

Reference is made to the brief (paper number 20) and the answer (paper number 21) for the respective positions of the appellant and the examiner.

OPINION

For all of the reasons expressed by the appellant, and for the additional reasons set forth infra, we will reverse the 35 U.S.C.

§ 103(a) rejection of claims 15 and 18 through 36.

¹ The examiner refers to this reference by the assignee, Matsushita (answer, page 3).

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The examiner's rejection (answer, page 3) reads as follows:

Japan '342 in figure 3 [sic, figure 1] discloses a substrate having semiconductive regions 29 on active device regions defined by trench regions 25 and planar with trench fill material 28 in the trenches on substrate. It would have been within the scope of one of ordinary skill in the art to form the regions such that they are of different thicknesses or such that they are doped with different dopant atoms or to different concentrations in formation of a BiCMOS device in view of the motivation provided by Eklund to form a BiCMOS device having regions of different dopant types and concentrations as well as thicknesses and the motivation provided by Jastrzebski to form different semiconductive regions selectively by masking regions of a substrate, growing a semiconductive region and then masking the semiconductive region and growing another semiconductive region on the substrate.

We agree with the appellant that: Yoneda discloses "a method of forming a deep insulator separation in a semiconductor integrated circuit by forming a second groove [30] on a first groove [25] formed on a semiconductor substrate [20], and burying the second groove to form an interelement separating region" (brief, page 5); Eklund discloses "the use of silicon on insulator ("SOI") technology for making a bipolar transistor structure on a buried oxide layer which may be incorporated into a method for fabricating bipolar transistors in a BiCMOS structure" (brief, page 7); Eklund teaches away from trench

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isolation (brief, page 8; column 1, lines 43 through 51; and column 3, lines 13 through 18); Jastrzebski discloses "a method of forming a CMOS FET structure by forming an apertured insulating layer on a silicon substrate" and forming first and second monocrystalline silicon islands of opposite conductivity types adjacent to each other (brief, pages 8 and 9); and Jastrzebski "distinguishes his invention from both trench isolation technologies and SOI technologies" (brief, page 9; column 1, line 32 through column 2, line 36). We likewise agree with the appellant's conclusion (brief, page 9) that:

In the present instance, the cited references clearly lead away from each other. Absent the impermissible use of hindsight reconstruction based on applicant's own disclosure, one skilled in the art would find no suggestion to combine them.

Even if we assume for the sake of argument that the references could somehow be combined, the claimed invention still would not be met by the combined teachings. Thus, the 35 U.S.C. § 103(a) rejection of claims 15 and 18 through 36 is reversed.

DECISION

The decision of the examiner rejecting claims 15 and 18 through 36 under 35 U.S.C. § 103(a) is reversed.

REVERSED

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KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
JOSEPH F. RUGGIERO)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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Letty

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APPEAL NO. 1999-1576

APPLICATION NO. 08/347,527

APJ HAIRSTON

APJ GROSS

APJ RUGGIERO

DECISION: **REVERSED**

PREPARED: Nov 6, 2002

OB/HD

PALM

ACTS 2

DISK (FOIA)

REPORT

BOOK