

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 23

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte LEE-LEAN SHU,
KURT KNORPP, and KATSUNORI SENO

Appeal No. 1999-1126
Application No. 08/722,486

HEARD: March 20, 2001

Before THOMAS, KRASS, and BARRY, Administrative Patent Judges.
BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the rejection of claims 4, 5, 12, and 13. We reverse.

BACKGROUND

The invention at issue in this appeal relates to static random access memories (SRAMs). An increase in the size and storage capacity of SRAMs has made it difficult to generate and distribute short duration clock pulses on a large scale for large, high-speed SRAMs. Although such clock pulses

conventionally have been required to equalize bit lines in an SRAM, the use of the pulses prolongs access times and degrades overall performance of the SRAM.

The appellants' SRAM employs a current mode data path to overcome the aforementioned shortcomings. More specifically, their SRAM uses two cascade complementary differential current amplifiers in a readout circuit. The amplifiers employ special bias circuits and provide improved amplifier operation. Advantageously, a small amplifier differential input resistance reduces the voltage swing of differential lines thereby eliminating the need for equalization clocks. The unique bias circuit of the claimed invention improves operation of the amplifiers and allows the amplifiers to be used in differential cascaded applications such as in an SRAM read data path.

Claim 12, which is representative for our purposes, follows:

12. A semiconductor memory comprising a plurality of memory cells arranged in rows and columns at least one two stage differential current

sensing amplifier having a pair of input terminals connected to a pair of bit lines, said differential current sensing amplifier having a pair of input transistors connected to said bit line pair and means for biasing said input transistors into conduction, and wherein neither of said input transistors is cut off during reading or writing access to said memory.

The references relied on in rejecting the claims follow:

Sasaki et al. (Sasaki) 1992	5,126,974	June 30,
		(filed Jan. 16, 1990)
Nogle et al. (Nogle) 1993	5,229,967	July 20,
		(filed Sep. 4, 1990)
Taguchi 1994	5,339,273	Aug. 16,
		(filed Dec. 13, 1991).

Claims 4, 5, 12, and 13 stand rejected under 35 U.S.C. § 102(e) as anticipated by Taguchi. Claims 4, 12, and 13 stand rejected under § 102(e) as anticipated by Sasaki or Nogle. Claim 5 stands rejected under 35 U.S.C. § 103(a) as obvious over Sasaki or Nogle. Rather than repeat the arguments of the appellants or examiner in toto, we refer the reader to the brief and answer for the respective details thereof.

OPINION

In deciding this appeal, we considered the subject matter on appeal and the rejection advanced by the examiner. Furthermore, we duly considered the arguments and evidence of the appellants and examiner. After considering the record, we are persuaded that the examiner erred in rejecting claims 4, 5, 10, and 12. Accordingly, we reverse.

We begin by noting the following principles from Rowe v. Dror, 112 F.3d 473, 478, 42 USPQ2d 1550, 1553 (Fed. Cir. 1997).

A prior art reference anticipates a claim only if the reference discloses, either expressly or inherently, every limitation of the claim. See Verdegaal Bros., Inc. v. Union Oil Co., 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "[A]bsence from the reference of any claimed element negates anticipation." Kloster Speedsteel AB v. Crucible, Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

With these principles in mind, we address the appellants' arguments and the examiner's responses.

The appellants' argue, "the Taguchi reference does not set forth or suggest a device wherein a differential current sensing amplifier is employed" (Appeal Br. at 4.) They

further argue, "neither Sasaki nor Nogle provide any teaching or suggestion whatsoever regarding the claimed differential current sensing amplifier" (Id. at 6.) The examiner responds, "[i]t also would have been obvious to use any other types of amplifiers as amplifier of Taguchi, Sasaki or Nogle in order to detect voltage or current on the bit lines."
(Examiner's Answer at 5.)

Claims 4, 5, 12, and 13 specify in pertinent part the following limitations: "at least one two stage differential current sensing amplifier" Accordingly, the limitations require a differential current sensing amplifier.

The examiner fails to show a teaching of the limitations in Taguchi, Sasaki, or Nogle. Although Taguchi discloses a sense amplifier (SA), the SA is not a differential current sensing amplifier. To the contrary, the SA amplifies a voltage difference between bit lines. Specifically, the "sense amplifier **SA** amplifies a voltage difference of bit lines **BL1** and **BL1X** of the cell array **CAR1** or a voltage

difference of bit lines **BL2** and **BL2X** of the cell array **CAR2**." Col. 5, ll. 1-4.

Although Sasaki discloses a sense amplifier circuit, the circuit is not a differential current sensing amplifier. To the contrary, the circuit amplifies a voltage difference between output signals. "[S]pecifically, the invention relates to a sense amplifier circuit technology integrated with the memory cells to amplify a pair of complementary signals having a minute potential difference¹ and read out from a memory cell." Col. 1, ll. 5-7.

Similarly, although Nogle teaches a sense amplifier, the amplifier is not a differential current sensing amplifier. To the contrary, the amplifier employs a voltage difference. Specifically, "[t]he sense amplifier provides a first differential current between the positive and negative output terminals proportional to a difference in voltage between the

¹A potential difference is "the voltage difference between two points" Webster's Ninth New Collegiate Dictionary 921 (1990) (emphasis added).

positive and negative input terminals when either a voltage on the positive input terminal or a voltage on the negative input terminal exceeds a predetermined voltage." Col. 1, l. 64 - col. 2, l. 2.

Because Taguchi merely teaches amplifying a voltage difference between bit lines, Sasaki teaches amplifying a voltage difference between output signals, and Nogle teaches employing a voltage difference, we are not persuaded that any of the references discloses the limitations of "at least one two stage differential current sensing amplifier"

Because the rejections of the independent claims are for anticipation, the examiner's allegation about the obviousness of using other types of amplifiers in the references is irrelevant. Furthermore, he fails to provide evidence to support his allegation that "[a] current sense amplifier and a voltage sense amplifier are interchangeably usable in a semiconductor memory device." (Examiner's Answer at 5.) Therefore, we reverse the rejection of claims 4, 5, 12, and 13 as anticipated by Taguchi; the rejection of claims 4, 12, and

13 as anticipated by Sasaki or Nogle; and the rejection of claim 5 as obvious over Sasaki or Nogle.

CONCLUSION

In summary, the rejections of claims 4, 5, 12, and 13 under 35 U.S.C. § 102(e) and of claim 5 under 35 U.S.C. § 103(a) are reversed.

REVERSED

JAMES D. THOMAS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
ERROL A. KRASS)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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)	
LANCE LEONARD BARRY)	
Administrative Patent Judge)	

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MELVIN A. ROBINSON
HILL, STEADMAN & SIMPSON
A PROFESSIONAL CORPORATION
85TH FLOOR SEARS TOWER
CHICAGO, IL 60606