

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ICHIRO MIYANO, KOJI SERIZAWA, HIROYUKI TANAKA,
TADAO SHINODA and SUGURU SAKAGUCHI,

Appeal No. 1999-0884
Application No. 08/464,577

HEARD: April 3, 2001

Before BARRETT, FLEMING and BARRY **Administrative Patent Judges**
FLEMING, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 6-9 and 24-43, the only claims pending in the application.

The invention relates to a method for forming a film carrier tape for a semiconductor device, and for forming a laminated multi-chip semiconductor device that includes a

plurality of chip semiconductor devices stacked in multiple layers on a substrate.

The method of forming a film carrier tape comprises the steps of superposing a metallic layer on a carrier member (page 6, lines 13-16) and etching the metallic layer so as to form metallic leads (page 6, lines 16-18) and a heat sink (page 6, lines 19-28) separate from the metallic leads. The heat sink is to be formed in a direction transverse to that in which the metallic leads extend (page 6, lines 19-28; Figs. 1 and 2). The metallic leads are connected to the semiconductor chip and/or a connector therefor (page 7, lines 4-6), and the heat sink is coupled to the semiconductor device to radiate heat therefrom (page 6, lines 23-28).

The method of forming a multi-chip semiconductor device comprises the steps of providing a film carrier tape with leads (page 6, lines 11-13), electrically connecting a semiconductor chip to the leads of the film carrier tape (page 7, lines 4-7), mounting a heat sink to a surface of the semiconductor chip

(page 7, lines 7-11), and providing a connector for the mounting of the heat sink (page 7, line 26 to page 8, line 8). The film carrier tape has a superimposed metallic layer, which is etched to form the leads and heat sink for the semiconductor chip

(page 6, lines 16-23); the metallic leads extend in a first direction, and the heat sink extends in a second direction transverse to the first (page 6, lines 19-28; see Figs. 1 and 2). At least one positioning mark is provided on the heat sink

(page 7, line 28 to page 8, line 8), and a corresponding mark is provided on the connector, corresponding to the first mark. A heat conducting pattern is formed on the substrate (page 9, lines 1-17), and the heat sink is connected to the substrate through the conducting pattern. An opening may be provided in the heat sink (page 10, lines 3-11), overlaying the semiconductor chip. Radiation fins may be provided at an outer exposed portion of the heat sink (page 12, lines 6-9). A heat insulator may be provided between adjacent ones of the semiconductor chip devices to

reduce heat transfer between them (page 12, line 22 to page 13, line 23).

Independent claims 6 and 24 are reproduced as follows:

6. A method for forming a film carrier tape for a semiconductor device comprising the steps of superposing a metallic layer on a carrier member and etching the metallic layer so as to form metallic leads and a heat sink separate from the metallic leads for the semiconductor device.

24. A method of forming a laminated multi-chip semiconductor device comprising a step of stacking a plurality of chip semiconductor devices in multiple layers on a substrate, wherein said chip semiconductor devices are formed by the steps of:

providing a film carrier tape with leads;

electrically connecting a semiconductor chip to the leads of the film carrier tape;

mounting a heat sink separate from the leads electrically connected to the semiconductor chip to a surface of the semiconductor chip; and

providing a connector for the mounting of the heat sink and electrically connecting the connector to the leads of the film carrier tape.

The Examiner relies on the following references:

Takahashi et al. (Takahashi)	4,315,845	Feb. 16, 1982
Kuraishi	4,809,053	Feb. 28, 1989
Kitano et al. (Kitano)	5,047,837	Sep. 10, 1991 (filed Aug. 03, 1989)
Sugano et al. (Sugano)	5,198,888	Mar. 30, 1993 (filed Dec. 20, 1990, a divisional of 07/288,955,

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U.S. Patent No. 5,028,986, filed Dec. 23, 1988)

Otaka¹ JP 61-80842 Apr. 24, 1986

Claims 6-9, 24-28, 30, 32-35 and 37-43 stand rejected under 35 U.S.C. § 103 as being unpatentable over Sugano in view of Kitano. Claim 29 stands rejected under 35 U.S.C. § 103 as being unpatentable over Sugano, Kitano, and Takahashi. Claim 31 stands rejected under 35 U.S.C. § 103 as being unpatentable over Sugano, Kitano, and Kuraishi. Claim 36 stands rejected under 35 U.S.C. § 103 as being unpatentable over Sugano, Kitano, and Otaka.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the brief and the answer for the details thereof.

OPINION

We will not sustain the rejection of claims 6-9 and 24-43 under 35 U.S.C. § 103.

¹A copy of the translation provided by the U.S. Patent and Trademark Office on March 26, 2001, is included and relied upon in this decision.

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The Examiner has failed to set forth a *prima facie* case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. *In re Sernaker*, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." *Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.*, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), *cert. denied*, 117 S.Ct. 80 (1996) *citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984).

On pages 22-23 of the Brief, Appellants argue that Sugano does not teach etching the metallic layer to form a heat sink separate from the metallic leads for the semiconductor devices.

Further, Appellants contend that Kitano is directed to a lead

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frame type of device, in which the heat sink is formed by punching from a single sheet material, and is therefore completely different from the film carrier TAB type of device. Appellants therefore conclude that the combination proposed by the Examiner would not have resulted in the claimed invention. Further, Appellants assert, even assuming the combination of Sugano and Kitano teaches every element of the claimed invention, the person having ordinary skill in the art would not have found it obvious to make the combination advanced by the Examiner.

In the answer, the Examiner admits that Sugano does not teach etching a heat sink, but asserts that Kitano teaches a process comprising the steps of forming a metallic layer to form leads and a heat sink, as claimed in claim 6. The Examiner offers evidence to show that the process of Kitano is a "one-layer TAB tape."

As pointed out by our reviewing court, we must first determine the scope of the claim. "[T]he name of the game is the claim." *In re Hiniker Co.*, 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).

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Appellants' claim 6 recites a method of forming a film carrier tape for a semiconductor device, comprising the steps of superposing a metallic layer on a carrier member and etching the metallic layer to form (a) metallic leads and (b) a heat sink separate from the metallic leads.

Upon a careful review of Sugano and Kitano, we fail to find that these references teach the step of etching the metallic layer on a carrier member to form both metallic leads and a heat sink separate from the metallic leads, as claimed in independent claim 6. We agree with the Examiner that Sugano teaches forming a film carrier tape, superposing a metallic layer on the carrier member, and etching the metallic layer so as to form metallic leads (see column 5, lines 29-34). We agree that Kitano teaches a heat sink 7, having radiation fins in some embodiments, contacting a semiconductor chip so as to radiate heat away from the chip (see column 5, line 67 to column 6, line 2). Neither reference, however, teaches etching the metallic layer on a carrier member to form such a heat sink. The Examiner admits that Sugano does not teach a heat sink. Appellant asserts that the "heat transfer cap" of Kitano is not etched from a metallic layer, but rather

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punched out of sheet metal; while the detailed

description in Kitano is silent as to the method of forming the heat transfer cap, the drawings suggest that the heat transfer cap is punched, just as the chip pad 2 is punched (see, for example, Figs. 1-3), and the Examiner does not contravene Appellants' assertion that Kitano's heat sink is punched. We therefore find that the heat transfer cap of Kitano is not formed by etching a metallic layer. Because neither Sugano nor Kitano teaches a heat sink formed by etching a metallic layer, the combination advanced by the Examiner does not contain every element of the invention recited in claim 6.

Appellants' claim 24 recites a method of forming a laminated multi-chip semiconductor device comprising stacking a plurality of chip semiconductor devices in layers on a substrate, (each) chip semiconductor device formed by the steps of electrically connecting a chip to the leads of a film carrier tape, mounting a heat sink to a surface of the semiconductor chip, separate from those connected leads, and electrically

connecting a heat sink connector to the leads of the film carrier tape.

Upon a careful review of Sugano and Kitano, we fail to find that these references teach a stacked multi-chip structure in which each chip has an associated heat sink for radiating away

generated heat. We agree with the Examiner that Sugano teaches stacking a plurality of chip semiconductor devices 15a-c in layers on a substrate 20, each device formed by electrically connecting the chip to a film carrier tape 2a having leads 3a. As noted *supra*, the Examiner admits that Sugano does not teach a heat sink, but advances Kitano as teaching a heat sink. We note that claim 24, unlike claim 6, does not require that the heat sink be etched from a metallic layer. Nevertheless, Kitano does not supply the missing teaching, because the heat transfer cap contained in Kitano contacts only the upper chip of a semiconductor device structure. Neither Sugano nor Kitano teaches a stacked multi-chip semiconductor device provided with a heat sink or sinks such that each semiconductor chip is in thermal contact with a

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heat sink. Therefore, the combination advanced by the Examiner fails to teach every element recited in claim 24.

Appellants' Claim 37 recites a method of forming a laminated multi-chip semiconductor device. Many limitations are very similar to those contained in claim 24; in particular, claim 37 recites "for at least an intermediate layer of the at least three layers of the chip semiconductor devices ... providing a heat sink separate from the leads electrically connected to the

semiconductor chip at a surface of the semiconductor chip for enabling heat radiation therefrom." As noted, *supra*, in the discussion of claim 24, neither Sugano nor Kitano teaches a stacked multi-chip semiconductor device provided with a heat sink or sinks so that each semiconductor chip is in thermal contact with a heat sink. Therefore, the combination advanced by the Examiner fails to teach every element recited in claim 37.

Claims 7-9, 25-36, and 38-43 depend from independent claims 6, 24, and 37, respectively, and incorporate every limitation of the independent claim from which they depend.

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For the reasons expressed, *supra*, we find that the combinations advanced by the Examiner fail to teach every element recited in these claims.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." ***Para-Ordnance***, 73 F.3d at 1087, 37 USPQ2d at 1239,

citing W. L. Gore & Assocs., 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13.

Upon a review of the references relied upon by the Examiner, we fail to find any suggestion or reason to etch the metallic layer formed on a carrier member to form a heat sink

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along with, and separate from, metallic leads to be connected to a semiconductor device; we further fail to find any suggestion or reason to form a stacked multi-chip semiconductor structure wherein a heat sink is mounted to the surface of each chip in the stack. Sugano does not suggest the desirability of providing a heat sink or sinks to radiate heat from the TAB type multi-chip structure disclosed. Kitano teaches a heat sink for a chip semiconductor device, but does not suggest the desirability of forming such a heat sink by etching; neither does Kitano suggest placing each chip in a stacked multi-chip structure in thermal contact with an associated heat sink. Takahashi, Otaka and Kuraishi were not relied upon by the Examiner to teach process steps for forming or constructing heat sinks, and in any case do not teach or suggest the elements missing from Sugano and Kitano.

Therefore, we will not sustain the rejection of claims 6-9 and

24-43 under 35 U.S.C. § 103(a) as being unpatentable over Sugano, Kitano, Takahashi, Otaka, and Kuraishi.

In view of the foregoing, the decision of the Examiner

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rejecting claims 6-9 and 24-43 under 35 U.S.C. § 103, is
reversed.

REVERSED

LEE E. BARRETT)	
Administrative Patent Judge)	
)	
)	
)	BOARD OF PATENT
MICHAEL R. FLEMING)	APPEALS AND
Administrative Patent Judge)	INTERFERENCES
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