

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board

Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KAZUO TOMITA,
SHIGENORI SAKAMORI
and HIROSHI KIMURA

Appeal No. 1999-0874
Application 08/726,733

ON BRIEF

Before THOMAS, FLEMING and DIXON, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellants have appealed to the Board from the examiner's final rejection of claims 1-13.

Representative claim 1 is reproduced below:

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1. A semiconductor device having a conductive contact layer structure, comprising:

first conductive layers formed on a main surface of a semiconductor substrate with an insulating film therebetween;

a conductive region formed under and between said first conductive layers in the main surface of said semiconductor substrate;

a first insulation layer formed on said first conductive layers, having a first hole reaching a surface of said conductive region;

a second insulation layer formed on said first insulation layer with a high etching selectivity with respect to said first insulation layer, having a second hole in communication with said first hole;

a sidewall insulation film formed at an inner sidewall of said second insulation layer defining said second hole; and

a second conductive layer formed inside said first and second holes so as to be electrically connected to said conductive region and to be electrically insulated from said first conductive layer.

The following references are relied on by the examiner:

Teng et al. (Teng)	4,656,732	Apr. 14, 1987
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Appellants' admitted prior art Figures 38 and 39

The following references are relied upon by the Board in its formulation of a new rejection in accordance with 37 CFR § 1.196(b):

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Kirk-Othmer, "Encyclopedia of Chemical Technology," Volume 13, Third Edition, pages 637-640 (1981)

Muller, "Device Electronics for Integrated Circuits," Second Edition, pages 96-98 (1986)

Claims 1-13 stand rejected under the second paragraph of 35 U.S.C. § 112.

Claims 7-13 also stand rejected under 35 U.S.C. § 102(b) as being anticipated by appellants' admitted prior art in Figures 38 and 39. Finally, claims 1-6 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon appellants' admitted prior art Figures 38 and 39 in view of Teng.

Rather than repeat the positions of the appellants and the examiner, reference is made to the briefs and the answer for the respective details thereof.

OPINION

Turning first to the rejection of claims 1-13 under the second paragraph of 35 U.S.C. § 112, it is to be noted that to comply with the requirements of the cited paragraph, a claim must set out and circumscribe a particular area with a reasonable degree of precision and particularity when read in light of the disclosure and the teachings of the prior art as it would be by the artisan. Note In re Johnson, 558 F.2d 1008, 1016, 194 USPQ 187, 194 (CCPA 1977); In re Moore, 439 F.2d 1232, 1235, 169 USPQ 236, 238 (CCPA 1971).

We have reviewed and considered the examiner's reasons in support of the rejection, but are not convinced that the cited claims fail to comply with the second paragraph of 35 U.S.C. § 112. The examiner's view is first expressed at page 4 of the answer that it is not clear from the figures that the claimed "first insulating layer" is formed on the first conductive layer. As amplified at page 6 of the answer, the examiner considers the term "on" to mean direct contact. The examiner thus concludes from the figures there is no direct contact between the first insulating layer (9,10) and the conductive layers (4).

The examiner's views expressed in the answer are not consistent with the disclosed invention in accordance with the correlation by appellants in Exhibit A to the principal brief on appeal showing representative corresponding structural elements for each element claimed in independent claims 1 and 7 on appeal and the discussion beginning at page 24 of the specification as filed. Therefore, in accordance with the above noted case law, the artisan would not construe the questioned claim language in the manner consistent with the examiner's view that the use of word "on" requires direct contact in this case. Not only do we understand the artisan would view this term as permitting an intermediate insulation layer 5 between the identified first insulating layer (paired layers 9 and 10), but also from our own understanding of the integrated circuit art, the artisan would not so construe the claim as necessarily requiring the recited element be placed directly on another element. This later view is consistent with the

factual findings of basic technology of MOS field-effect transistors made by Judge McKelvie in Thorn EMI North America, Inc. v. Intel Corp., 928 F.Supp. 449, 450-51 (D. Del. 1996), affirmed, 157 F.3d 887, 48 USPQ2d 1181 (Fed. Cir. 1998). The claimed invention recited in independent claims 1 and 7 on appeal is consistent with the disclosed invention and would therefore not cause the artisan to misconstrue or otherwise not be readily able to determine the metes and bounds of the claimed invention within the second paragraph of 35 U.S.C. § 112. Therefore, the decision of the examiner rejecting claims 1-13 under that statutory provision is reversed.

We must also reverse the examiner's rejection of claims 7-13 under 35 U.S.C. § 102 as being anticipated by appellants' disclosed prior art Figures 38 and 39 based on the interpretation set forth at pages 6 and 7 of the answer. The examiner's views expressed there make no mention of the requirement of claim 7 that the second insulation layer formed on the first insulation layer must have a "high etching selectivity with respect to said first insulation layer."

According to the examiner's view, the claimed first insulation layer is layer 5 in Figures 38 and 39. The actual disclosed material in prior art Figures 26-39 is not identified as to what this insulation material actually comprises. On the other hand, the second insulating layer identified by the examiner in accordance with the rejection is layer 9, which is identified as silicon oxide by the disclosed prior art in the specification

as filed. Initially, it is thus clear that without an identified material of the first insulation layer there can be no meaningful relative etching selectivity that may be determined according to the examiner's views. Moreover, the art generally would have regarded such a general statement that layer 5 be insulating as being formed of silicon oxide like the material used to form the second claimed insulating layer 9 according to the examiner's view. Even in this scenario, there would be no relative differential etching selectivity between the two layers because they would be of the same material. When all these factors are considered, even if we were to agree with the examiner's views with respect to the other elements of claim 7 on appeal, the rejection must be reversed of independent claim 7 and its dependent claims.

For similar reasons, we reverse the rejection of claim 1 and its dependent claims 2 through 6 under 35 U.S.C. § 103 based upon the examiner's views of appellants' admitted prior art Figures 38 and 39 in view of Teng. The examiner has taken the same views with respect to Figures 38 and 39 as with the rejection of claims 7-13 under 35 U.S.C. § 102. Therefore, essentially for the same reasons we reverse the rejections of claims 1-6.

On the other hand, under the provisions of 37 CFR 1.196(b), we reject claims 1-13 under 35 U.S.C. § 103. As evidence of obviousness, we rely upon the corresponding figures of appellants' admitted prior art Figures 32-39 in view of Teng, further in view of Muller and Kirk-Othmer.

Treating independent claim 7 first, the claimed first conductive layer comprises gate electrode 4. The conductive region claimed corresponds to the diffused drain regions 6, 8. The first insulation layer comprises silicon oxide layer 9 on top of which is silicon nitride layer 10. The diameter of the first hole comprises the width extending between the diffused regions 6 just above the diffused region 8.

The claimed second insulation layer comprises silicon oxide layer 11. At this level of the vertically integrated structure of Figures 38 and 39, it is seen that the hole 110 has a larger diameter as claimed than the one just described with respect to the surface diffused regions 6, 8 corresponding to the first hole, thus meeting also the recitation of claim 7 that the second hole be larger than the first hole.

The use of sidewall oxides in vertical integration techniques for integrated circuits is detailed in Teng to aid in patterning contact holes, which techniques are directly applicable to the hole diameters and the function of the chip surface contact to the claimed second conductive layers of polysilicon 17 and tungsten silicide 18 in prior art Figures 38 and 39. The problems associated with the formation of the prior art structures between Figures 38 and 39 of the appellants' admitted prior art involve the desirability of placing circuit elements such as the gate electrodes 4 in Figure 36 closer together in Figure 37 compared to Figure 36, thus increasing the integrated circuit density of active circuit elements. This same consideration drives the disclosure in Teng from the initial paragraphs at column 1 of this reference.

As specifically applicable to independent claim 7, the discussion at column 5, lines 45-63 of Teng indicates to the artisan that silicon nitride would have had a relatively lesser etching rate than the silicon oxide in the interlevel dielectric discussed. Thus, in accordance with the feature of the second insulation level having a higher etching selectivity with respect to the first insulation layer, the silicon oxide layer discussed in this portion of Teng would have a higher etching selectivity as suggested by this discussion than the silicon nitride layer. These are the same corresponding materials associated with the claimed first insulation layer and the second insulation layer in appellants' representative prior art Figures 38 and 39.

Moreover, in discussing the formation of insulating films such as silicon dioxide and silicon nitride beginning at the bottom of page 96 of Muller, the statement is made at the top of page 97 that silicon nitride layers do not oxidize as readily as do silicon oxide layers. This suggests again relative, selective etching or oxidation capabilities between the two materials. Selective oxidation is specifically taught at the top of page 638 of the section of Kirk-Othmer indicating that silicon nitride is an ideal material for such selective oxidation since it too has an extremely slow rate of oxidation. The discussion at the top of page 639 indicates that the selection of relative etch rate selectivity is important in the fabrication of integrated circuit structures and may for example be controlled by the nature of the etching material such as in corresponding Table 3 at page 640. This table indicates that silicon dioxide and silicon nitride may

have somewhat corresponding etch rates but different etch rates with respect to different etchants, which are beyond apparatus claims 1-13 on appeal. Collectively taken then, the teachings and suggestions in Teng, Muller and Kirk-Othmer indicate that the materials comprising claimed second insulation layer, corresponding to silicon oxide layer 11 of appellants' prior art Figure 38 and 39, would have a correspondingly or relatively higher etch rate than the claimed first insulation layer, correspondingly comprising the silicon nitride layer 10 in prior art Figures 38 and 39.

As to independent claim 1 on appeal, this claim does not recite the relative hole size as independent claim 7 does, but does recite that a sidewall insulation layer exists at an inner sidewall of the second insulation layer defining the second hole, in contrast to independent claim 7 on appeal. The bulk of the teachings in Teng apply to this feature such as is shown in Figure 2C, Figure 4 and Figure 6C as relied upon by the examiner. Since the hole size in claim 1 may be the same or even reversed from that recited in independent claim 7 on appeal, the teaching value of Teng is pertinent. The most succinct statement of the teachings of this reference appear to be in the first paragraph at column 3. The discussion in the initial paragraphs of column 5 are also pertinent to the point of indicating that the use of the techniques in Teng allow for "sublithographic hole sizes that are smaller than could be directly patterned with normal lithographic techniques." Note column 5, lines 29-32. Various advantages are discussed at columns 6 and 7 including in the paragraph bridging these columns that

short circuits may be avoided following Teng with the additional teaching value at column 7 that more compact layouts may be obtained. These teachings directly address the problems of appellants' admitted prior art Figures 38 and 39 as discussed in the paragraph bridging pages 7 and 8 of the specification.

Since the rejection is in part based upon the prior art structure of appellants' admitted prior art Figures 38 and 39, on which the disclosed invention in appellants' invention in Figures 1 and 7 are in turn based, the subject matter of the dependent claims 2-6 and 8-13 would clearly have been obvious to the artisan as well. The bulk of the features recited in these dependent claims appear to be substantially identical but with different claim dependencies. What defines a hole diameter appears to be somewhat arbitrarily determinable and therefore obvious, and the relative hole diameters and the number of them appear to be a function of the etchants and the number of vertically chosen layers to integrate.

In view of the foregoing, we have reversed the examiner's rejection of claims 1-13 under the second paragraph of 35 U.S.C. §112. We have also reversed the rejection of claims 7-13 under 35 U.S.C. §102 and the separate rejection of claims 1-6 under 35 U.S.C. §103. In contrast, however, we have instituted a new ground of rejection in accordance with the provisions of 37 CFR §1.196(b) of all claims on appeal, claims 1-13, under 35 U.S.C. §103. Therefore, the decision of the examiner is reversed.

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This decision contains a new ground of rejection pursuant to 37 CFR § 1.196(b). 37 CFR § 1.196(b) provides that, “A new ground of rejection shall not be considered final for purposes of judicial review.”

37 CFR § 1.196(b) also provides that the appellants, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of proceedings (§ 1.197(c)) as to the rejected claims:

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(1) Submit an appropriate amendment of the claims so rejected or a showing of facts relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the application will be remanded to the examiner. . . .

(2) Request that the application be reheard under § 1.197(b) by the Board of Patent Appeals and Interferences upon the same record. . . .

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

REVERSED
37 CFR § 1.196(b)

James D. Thomas)	
Administrative Patent Judge)	
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)	
)	BOARD OF PATENT
Michael R. Fleming)	
Administrative Patent Judge)	APPEALS AND
)	
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