

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHUEN-DER LIEN

Appeal No. 1999-0866
Application No. 08/742,704

ON BRIEF

Before THOMAS, KRASS, and GROSS, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellant has appealed to the Board from the examiner's final rejection of claims 12 through 23, 35 through 38 and 55.

Representative claim 12 is reproduced below:

12. A process for forming an interconnect structure, comprising the steps of:

depositing a first conductive layer overlying one surface of a semiconductor substrate;

forming a first dielectric layer overlying said first conductive layer;

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forming a via in said first dielectric layer;

forming a first conductive plug within said via; and

selectively removing a first portion of said first conductive plug, a first portion of said first dielectric layer and a first portion of said first conductive layer thereby forming said interconnect structure, said interconnect structure comprising a first conductive lead formed by a second portion of said first conductive layer, a second conductive plug formed by a second portion of said first conductive plug and a second dielectric layer formed by a second portion of said first dielectric layer wherein said second conductive plug has an upper surface, a lower surface contacting an upper surface of said first conductive lead, a first side aligned with a side of said first conductive lead, a second side in contact with said second dielectric layer and a third side in contact with said second dielectric layer, said second side and said third side being adjacent to one another.

The following references are relied on by the examiner:

Brighton et al. (Brighton) 1991	4,996,133	Feb. 26,
Ozaki et al. (Ozaki) 1992	5,084,416	Jan. 28,
Ohshima 1995	5,420,074	May 30,

(filed Sep. 08,
1994)

Wolf, "Multilevel-Interconnect Technology For VLSI and ULSI," Silicon Processing For The VLSI ERA - Volume II: Process Integration, pp. 222-23, 253 (Sunset Beach, CA, Lattice Press, 1990).

Claims 12 through 23, 35 through 38 and 55 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the

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examiner relies upon Brighton as to claims 12 through 14, 17 through 23, 35, 36, 38 and 55, adding Wolf as to claims 15 and 37, adding Ozaki to Brighton as to claims 15 and 16 and adding Ohshima to the combination of Brighton and Wolf as to claim 16.

Rather than repeat the positions of the appellant and the examiner, reference is made to the brief and the answer.

OPINION

Because we find independent claim 12 indefinite within 35 U.S.C. § 112, second paragraph, we pro forma reverse the art rejections of the claims on appeal. Speculation and conjecture must be utilized by us and by the artisan inasmuch as the claims on appeal do not accurately reflect what the disclosed invention is. Note In re Steele, 305 F.2d 859, 862, 134 USPQ 292, 295 (CCPA 1962).¹

NEW REJECTION WITHIN 37 CFR § 1.196(b)

Claims 12 through 23, 35 through 38 and 55 are rejected

¹The reversal of the outstanding art rejections under 35 U.S.C. § 103 should not necessarily be construed as a reversal of these rejections on the merits. The prior art relied upon by the examiner may well be pertinent to properly definite claims within 35 U.S.C. § 112 as a whole.

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under the second paragraph of 35 U.S.C. § 112 because of the following defects we note with respect to independent claim 12 on appeal. Claim 12 recites the methodology of forming an interconnect structure by first depositing various layers, then selectively removing certain first portions of them, yielding an interconnect structure of the remaining or second portions thereof. This interconnect structure is stated to comprise three elements: a first conductive lead formed by a second portion of a first conductive layer, a second conductive plug formed by a second portion of the first conductive plug and a second dielectric layer formed by a second portion of the first dielectric layer. The claim ends with the wherein clause defining more specifically the second conductive plug and doing so by defining its various surfaces and sides. Based upon our study of the written description portion of the specification as well as its attendant drawing figures, the recitation of "a third side in contact with said second dielectric layer, said second side and said third side being adjacent to one another" cannot reasonably be discerned.

Appellant makes specific reference to this noted

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recitation of the wherein clause at the end of claim 12 beginning at the top of page 5 of the brief. Appellant attempts to read a portion of the wherein clause upon the Figure 3 showing in the disclosed invention. Whereas the claim defines a lower surface, a first side and a second side with respect to a showing in the Figure, there is no corresponding claimed third side depicted in the Figure 3 embodiment. The claim does not define the relationship of the recited elements exactly in the manner argued. The statement that the "opposite side of conductor 20A is in alignment with dielectric 22A" is shown but not necessarily consistent with the language of claim 12 on appeal. What appears to be argued here to distinguish over the showing in Brighton is not what is claimed. We conclude that claim 12, and by inference its dependent claims on appeal, are indefinite within 35 U.S.C. § 112, second paragraph.

In summary we have pro forma reversed all art rejections under 35 U.S.C. § 103 of the claims on appeal and instituted a new rejection of them under 35 U.S.C. § 112, second paragraph, within the provisions of 37 CFR § 1.196(b).

This decision contains a new ground of rejection pursuant

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to 37 CFR § 1.196(b)(amended effective Dec. 1, 1997, by final rule notice, 62 Fed. Reg. 53,131, 53,197 (Oct. 10, 1997), 1203 Off. Gaz. Pat. & Trademark Office 63, 122 (Oct. 21, 1997)).

37 CFR

§ 1.196(b) provides that "[a] new ground of rejection shall not be considered final for purposes of judicial review."

37 CFR § 1.196(b) also provides that the appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of proceedings (37 CFR § 1.197(c)) as to the rejected claims:

(1) Submit an appropriate amendment of the claims so rejected or a showing of facts relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the application will be remanded to the examiner

(2) Request that the application be reheard under § 1.197(b) by the Board of Patent Appeals and Interferences upon the same record

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

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REVERSED; 37 CFR § 1.196(b)

JAMES D. THOMAS)	
Administrative Patent Judge)	
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ERROL A. KRASS)	APPEALS AND
Administrative Patent Judge)	INTERFERENCES
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