

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 32

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MIZANUR M. RAHMAN, FRED C. SABERNICK, JEFF A. SPROUSE, MARTIN J. GROSZ, PETER FU, and RUSSELL M. RECTOR

Appeal No. 1999-0320
Application No. 08/426,751

ON BRIEF

Before URYNOWICZ, GROSS, and BLANKENSHIP, Administrative Patent Judges.

URYNOWICZ, Administrative Patent Judge.

DECISION ON APPEAL

This appeal is from the final rejection of claim 13, the only claim pending in the application.

The invention pertains to a request pipeline for coupling a microprocessor to a shared bus. Claim 13 reads as follows:

13. A request pipeline for pipelining requests from a microprocessor external to the microprocessor, the request pipeline comprising:

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request storage means, coupled between the microprocessor and a shared system bus, for storing at least two requests from the microprocessor, wherein the requests are directed at devices which are coupled to the microprocessor over the shared system bus;

associated storage means, coupled to the request storage means, for storing data associated with a request when said request is a request to write said data to a memory location specified in the request;

control logic means, coupled between the microprocessor and the shared system bus for indicating to the microprocessor that the request has been accepted by the device to which the request is directed, whether or not the device is ready to accept the request, so long as the request storage means is available to store the request; and

means for outputting a request from the request storage means to the shared system bus when the device to which the request is directed and the shared system bus are ready to accept the request.

The reference relied upon by the examiner is:

Bouchard et al. (Bouchard)	5,333,296	Jul. 26,
1994		

Claim 13 stands rejected under 35 U.S.C. § 103 as being unpatentable over Bouchard.¹

¹ Although the Sakai et al. patent (U.S. Patent No. 5,377,342) is relied on by the examiner to support the position on appeal (see page 4 in the answer, Paper No. 23), this reference does not appear in the statement of the above rejection. Where a reference is relied on to support a rejection, whether or not in a minor capacity, there is no

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The respective positions of the examiner and the appellants with regard to the propriety of this rejection are set forth in the examiner's answer (Paper No. 23) and the appellants' brief and reply brief (Paper Nos. 22 and 24, respectively).

OPINION

After consideration of the positions and arguments presented by both the examiner and the appellants, we have concluded that the rejection should not be sustained.

We agree with appellants that Bouchard does not teach or suggest control means "for indicating to the microprocessor that the request has been accepted by the device to which the request is directed, whether or not the device is ready to accept the request, so long as the request storage means is

excuse for not positively including the reference in the statement of the rejection. In re Hoch, 428 F.2d 1341, 1342 n.3, 166 USPQ 406, 407 n.3 (CCPA 1970). Accordingly, we have not considered the teachings of Sakai et al. in reviewing the merits of the examiner's rejection.

available to store the request."² The examiner relies on teachings of the reference at column 61, lines 42-50, and also column 68, lines 50-56. These teachings are that acknowledge line 20e of Figure 22 is asserted by the bus interface 21 to the CPU 10 in the cycle after it has received with no parity errors the write address which was driven by the CPU in a cycle (column 61), and that if parity is good and the address is recognized as being in interface chip 21, then acknowledge line 20e is asserted and the information is moved into holding registers in queues 339 and 340 (Figure 23) so that the latches 336 are free to sample the next cycle (column 68).

The portions of Bouchard's disclosure relied on by the examiner are not a teaching of the claimed subject matter nor do they suggest that subject matter because they have nothing to do with acceptance of a request by a device as defined in the claim and to which the request is directed. With respect to claim 13, CPU 10 of Bouchard is the processor and bus 11 is the shared system bus. Memories 12 and 16, and CPUs 28 of the

² In their brief, appellants' arguments are limited to this element of the claim.

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reference correspond to the devices of claim 13 because these elements are devices which are coupled to the microprocessor 10 over the shared bus 11. See Appendix to the brief, claim 13, lines 7 and 8. Acknowledge line 20e indicates that interface arbiter 21 has accepted or received with no parity error a request from the microprocessor. Line 20e does not indicate to microprocessor 10 that the request has been accepted by a device 12, 13 or 28 to which it has been directed, whether or not the device is ready to accept the request, so long as the request storage means is available to store the request.

Absent evidence, the examiner's alternate position at page 4 of the answer that "it is well known in systems designed as in Bouchard to include in some manner a way to acknowledge that the write was [sic:has] actually taken place" is not persuasive.

REVERSED

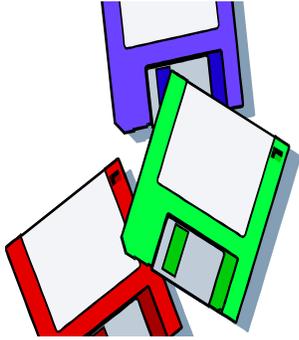
STANLEY M. URYNOWICZ)

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Administrative Patent Judge)	
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)	BOARD OF PATENT
ANITA PELLMAN GROSS)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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DECISION: REVERSED

Prepared: June 27, 2002

Draft Final

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