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Paper No. 10

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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***Ex parte*** STEVEN D. MILLMAN,  
MARKUS WLOKA and SEAN C. TYLER

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Appeal No. 1999-0259  
Application 08/596,857

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ON BRIEF

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Before FLEMING, RUGGIERO and BARRY, ***Administrative Patent Judges.***

FLEMING, ***Administrative Patent Judge.***

**DECISION ON APPEAL**

Appeal No. 1999-0259  
Application 08/596,857

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1-3, 10, 13 and 16-18. Claims 4-9, 14, and 15 stand objected to in the current application. Claims 11 and 12 are allowed.

The instant invention relates to a method of modeling a plurality of serially coupled circuit cells with a distributed serial load. Appellants' specification ("specification"), page 1, lines 5-8. The distributed serial load model is used in applications where the loading on one cell, e.g. cell 12, is affected by output loading on subsequent cells, e.g. cells 16, 18, and 20. Specification, page 9, lines 14-17. Cells 16-20 affect the loading on cell 12 because the input and outputs of cells 16-20 are transparent and unbuffered. Specification, page 9, lines 14-19. Since design rules do not require the input and output of each cell to be buffered, the loading on the one cell is affected by loading on the subsequent circuit cells, i.e. downstream loading is conveyed back to the first cell. Specification, page 10, lines 13-19. The effective load impedance of the unbuffered cells cannot be accurately modeled

by the typical single lumped capacitor. Specification, page 10, lines 21-23. The effective load impedance of these cells are more accurately modeled with an RC network (capacitor and resistor combination). Specification, page 3, line 37 to page 4, lines 1-2. One embodiment of the present invention features a data path having a plurality of serially coupled transmission gate cells. Specification, page 9, lines 25-30. In this embodiment, distributed serial load models the effective load impedance of the transmission gates with the RC network. Specification, page 10, line 8-12. Yet another embodiment of the present invention features a memory array comprising a plurality of bit cells within a WORDLINE. Specification, page 6, lines 30-34. WORDLINE is modeled with a distributed serial load and the RC load impedance network models the load of the bit cell. Specification, page 7, lines 15-21.

Appellants' independent claims encapsulate the various embodiments of the invention. The independent appealed claims 1, 10 and 16 are herein respectively recited:

1. A method of modeling loading of a plurality of serially coupled circuit cells, comprising the steps of:

identifying effective load impedances for each of the plurality of serially coupled circuit cells where the circuit cells include active elements; and

forming a distributed serial load with said effective load impedances where said distributed serial load provides a load model of the plurality of serially coupled circuit cells.

10. A method of simulating characteristics of a plurality of serially coupled circuit cells, comprising the steps of:

providing a first load for a first one of the plurality of serially coupled circuit cells where the circuit cells include active elements;

providing a second load for a second one of the plurality of serially coupled circuit cells where the circuit cells include active elements; and

forming a distributed serial load with said first and second loads of said first and second ones of the plurality of serially coupled circuit cells where said distributed serial load provides a characteristic load model of the plurality of serially coupled circuit cells.

16. A method of modeling a memory array comprising the steps of:

providing a first effective load impedance for a first bit cell of the memory array;

providing a second effective load impedance for a second bit cell of the memory array; and

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forming a distributed serial load with said first and second effective load impedances of said first and second bit cells where said distributed serial load provides a characteristic load model of the memory array.

In rejecting Appellants' claims, the Examiner relies on a single reference:

Komoda	5,379,232	Jan. 3,
1995		

Claims 1-3, 10, 13, and 16-18 stand rejected under 35 U.S.C. § 103 as being obvious over Komoda.

Rather than repeat the arguments of Appellants and Examiner, we refer the reader to the Appellants' Brief<sup>1</sup> and Examiner's Answer<sup>2</sup> for the respective details thereof.

#### **OPINION**

With full consideration being given the subject matter on appeal, the Examiner's rejection and the arguments

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<sup>1</sup>Appellants filed a Brief on Appeal ("Brief") on April 21, 1998.

<sup>2</sup>The Examiner, in response to Appellants' Brief, filed an Examiner's Answer on July 20, 1998.

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of Appellants and Examiner, for the reasons stated *infra*, we reverse the rejection of claims 1-3, 10, 13, and 16-18 under 35 U.S.C. § 103 as being unpatentable over Komoda.

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). *See also In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). The Examiner can satisfy this burden by showing that some objective teaching in the prior art or knowledge generally available to one

of ordinary skill in the art suggests the claimed subject matter. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Only if this initial burden is met does the burden of coming forward with evidence or argument shift to the Appellants. *Oetiker*, 977 F.2d at 1445, 24 USPQ2d at 1444. *See also Piasecki*, 745 F.2d at 1472, 223 USPQ at 788 ("After a *prima facie* case of obviousness has been established, the

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burden of going forward shifts to the applicant."). If the Examiner fails to establish a *prima facie* case, the rejection is improper and accordingly merits reversal. *Fine*, 837 F.2d at 1074, 5 USPQ2d at 1598.

We commence our analysis by reviewing and weighing all the pertinent evidence and arguments. *See Oetiker*, 977 F.2d at 1445, 24 USPQ2d at 1444 ("In reviewing the examiner's decision on appeal, the Board must necessarily weigh all of the evidence and argument.").

The Appellants' Arguments are directed to the three independent claims on appeal. In the discussion of claim 1, Appellants argue that "[they] have pointed to specific claim language in claim 1 . . . that distinguishes over the Komoda reference." *Brief* at pages 4-5. Specifically, Appellants assert that Komoda fails to teach the limitation "identifying effective

load impedances for each of the plurality of serially coupled circuit cells, where the circuit cells include active elements." *Brief* at pages 4-5. Next, in the discussion of

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claim 10, Appellants argue that Komoda fails to teach a similar limitation. "Again, at least the claim language 'providing a first load for a first one of the plurality of serially coupled circuit cells where the circuit cells include active elements' is not taught or suggested by Komoda."

**Brief** at page 6. Finally, in Appellants' discussion of Claim 16, Appellants argue that Komoda does not "teach or suggest modeling a bit cell memory array" where the bit cells include active elements. **Brief** at page 7.

The Examiner responds that Komoda "substantially" teaches all of the limitations of claim 1 and ". . . claims 10 and 16 are rejected based on the rejections of claim 1."

**Examiner's Answer** at page 4. However, although the Examiner agrees that Komoda does not specify that circuit cells include active elements, the Examiner rebuts that "[i]t would have been obvious to a person of ordinary skill in the art . . . [to] know [that] in a computer aided design and in . . . real time processing[,] active elements are standard means of design functions." **Examiner's Answer** at pages 4-5.

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First we must determine the scope of the claims. "[T]he name of the game is the claim." *In re Hiniker Co.*, 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998). In determining the scope of the independent claims on appeal, we focus on the disputed claim limitation "where the circuit cells include active elements." We construe the term "active elements" to ascertain its scope and meaning. *See In re Paulsen*, 30 F.3d 1475, 1480, 31 USPQ2d 1671, 1674. *The Modern Dictionary of Electronics* defines the term "active element [component]." The definition states:

1. Those components in a circuit that have gain, or direct current flow, such as SCRs, transistors, thyristors, or tunnel diodes. They change the basic character of an applied electrical signal by rectification, amplification, and switching and so forth. (Passive elements like inductors, capacitors, and resistors, have no gain characteristics).
2. A device, the output of which is dependent on a source of power other than the main input signal.
3. A device capable of some dynamic function (such as amplification, oscillation, signal control) and which usually requires an external power supply for its operation.
4. Broadly, any device (including electromechanical relay) that can switch (or amplify) by application of low-level signals.

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Rudolph F. Graf, *Modern Dictionary of Electronics* 10 (7th ed. 1999). Although all the definitions are suitable for our purposes, we rely on the fourth and broadest definition of the term, i.e. any device that can switch or amplify by application of low level signals.

It is well settled that “[c]laims must be read in view of the specification of which they are a part.” *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979, 34 USPQ2d 1321, 1329 (Fed. Cir. 1995. Appellants provide precise specification cites to support the amended claim language “that the circuit cells include active elements.” The specification, page 1, lines 16-24, reads in part:

The standard cell library includes a myriad of functional blocks such [as] NAND and NOR gates, multiplexers, memories, counters, multipliers, flipflops, etc. The standard cell can be as simple as an inverter and as complex as an arithmetic logic unit.

Further, the specification at page 3, lines 8-13, discloses in part:

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[A] circuit cell provides a predetermined logic function such as a NAND or NOR gate, inverter, flipflop, multiplexer, memory, counter, arithmetic logic unit, etc..

Finally, the specification at page 4, reads: "[a] circuit cell . . . is shown as [a] memory array . . . with a plurality of bit cells."

One of ordinary skill in the art knows or would be expected to know that memories, counters, flip-flops, and multipliers are circuit elements capable of producing a switching action in a circuit. So, Appellants' examples of circuit cells perfectly corresponds with *The Modern Dictionary of Electronics* definition of "active element [component]" as "any device that can switch or amplify."

Having determined the scope of Appellants' claims, we now turn to the Komoda teachings. Komoda teaches a wiring region dividing unit that receives a wiring layout (pattern) data. Komoda, column 3, lines 49-51. Komoda provides a circuit diagram

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showing an example of wiring layout data. Column 3, lines 49-51. The diagram "designates a wiring formed between an output of the inverter 21 and inputs of the inverters 22 and 23."

Komoda's circuit cell example of an inverter does not satisfy the definition of a circuit cell including an "active element." An inverter does not switch or amplify.

Additionally, Komoda's teaching of "wiring circuit data" (Komoda, column 4, line 4) would not suggest the use of an "active element" to one of ordinary skill in the art. Komoda does not otherwise separately teach or suggest the use of other circuit cells that may contain active elements.

The Examiner has not shown that Komoda teaches or suggests the limitation "where the circuit cells include active elements." Absent any such teaching or suggestion in Komoda, the Examiner's cursory rebuttal statement of obviousness ("[I]t would have been obvious to a person of ordinary skill in the art . . . [to] know [that] in a computer aided design and in . . . real time processing[,] active elements are standard means of design functions." Examiner's Answer at pages 4-5.)

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is unpersuasive and insufficient to support a conclusion of obviousness over Komoda.

The Federal Circuit instructs that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). It is further established that "[s]uch a suggestion may come . . . from the nature of the problem to be solved, leading inventors to look to references relating to possible solutions to that problem." ***Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc.***, 75 F.3d 1568, 1573, 37 USPQ2d 1626, 1630 (Fed. Cir. 1996), ***citing In re Rinehart***, 531 F.2d 1048, 1054, 189 USPQ 143, 149 (CCPA 1976)(considering the problem to be solved in a determination of obviousness). The Federal Circuit reasons in ***Para-Ordnance Mfg. Inc. v. SGS Importers Int'l Inc.***, 73 F.3d 1085, 1088-89, 37 USPQ2d 1237, 1239-40 (Fed. Cir. 1995), that for the

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determination of obviousness, the court must answer whether one of ordinary skill in the art who sets out to solve the problem and who had before him in his workshop the prior art, would have been reasonably expected to use the solution that is claimed by the Appellants. However, "[o]bviousness may not be established using hindsight or in view of the teachings or suggestions of the invention." *Para-Ordnance Mfg.*, 73 F.3d at 1087, 37 USPQ2d at 1239, *citing W.L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1551, 1553, 220 USPQ 303, 311, 312-13 (Fed. Cir. 1983). In addition, our reviewing court requires the Patent and Trademark Office to make specific findings on a suggestion to combine prior art references. *In re Dembiczak*, 175 F.3d 994, 1000-01, 50 USPQ2d 1614, 1617-19 (Fed. Cir. 1999).

Based on the evidence and arguments presented, and the pertinent law in this matter, we find that the Examiner has failed to establish a *prima facie* case of unpatentability with

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respect to independent claims 1, 10, and 16. Appellants' dependent claims 2-3, 13 and 17-18, the patentability of which were not argued separately, stand with the independent claims. ***In re Sernaker***, 702 F.2d 989, 991, 217 USPQ 1, 3 (Fed. Cir. 1983).

In view of the foregoing, we conclude that the Examiner has not established a ***prima facie*** case of unpatentability under 35 U.S.C. § 103 and therefore find the rejection of claims 1-3, 10, 13, and 16-18 improper. Accordingly, we reverse the Examiner's decision.

**REVERSED**

	MICHAEL R. FLEMING	)	
	Administrative Patent Judge	)	
		)	
		)	
		)	BOARD OF
PATENT		)	
	JOSEPH RUGGIERO	)	APPEALS AND
	Administrative Patent Judge	)	
INTERFERENCES		)	
		)	
		)	
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