

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SIMON A. SEGARS

Appeal No. 1999-0166
Application No. 08/656,544

ON BRIEF

Before RUGGIERO, BARRY, and LEVY, Administrative Patent Judges.

RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal from the final rejection of claims 1 and 3-9. Claim 2 has been canceled.

The disclosed invention relates to a data processing method and apparatus including an integrated circuit having a processor core and a scan chain in which the processor core executes instructions using either a system clock signal or a test clock signal. Clock selecting circuitry selects the

system clock signal during normal operation and the test clock signal during loading of program instructions during a test operation. During a test operation, the clock selecting circuitry is responsive to one or more clock selecting bits within a program instruction to select either the test clock signal or the system clock signal to drive the processor core to execute the program instruction.

Claim 1 is illustrative of the invention and reads as follows:

1. Apparatus for processing data, said apparatus comprising:

(i) a processor core operable under control of program instructions;

(ii) a clock circuit for supplying a system clock signal to said processor core;

(iii) a test clock circuit for supplying a test clock signal to said processor core;

(iv) a clock selector for selecting which one of said system clock signal and said test clock signal drives operation of said processor core; and

(v) an auxiliary circuit coupled to said processor core and driven by said system clock signal irrespective of which clock signal is selected for supply to said processor core by said clock selector, said auxiliary circuit being accessed by said processor core only when executing a program instruction from a subset of said program instructions;

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(vi) wherein said clock selector selects said system clock signal during normal operation and said test clock signal during loading of program instructions during test operation, said clock selector being responsive to one or more clock selecting bits within each program instruction to be executed during said test operation to select independently for each program instruction either said test clock signal or said system clock signal for driving said processor core to execute that program instruction, said clock selector selecting said system clock signal to drive operation of said processor core during test operation to execute a program instruction from said subset of program instructions such that operation of said processor core is synchronized with said auxiliary circuit.

The Examiner relies on the following prior art:

Antanaitis, Jr. et al.	5,163,146	Nov. 10, 1992
(Antanaitis)		
Greenberger et al.	5,355,369	Oct. 11, 1994
(Greenberger)		(filed Apr. 26, 1991)
Sakai et al. (Sakai)	5,479,645	Dec. 26, 1995
(filed Oct. 07, 1992)		
Ganapathy	5,561,792	
Oct. 01, 1996		(effectively filed Dec. 28, 1992)

Claims 1 and 3-9 stand finally rejected under 35 U.S.C. § 103. As evidence of obviousness, the Examiner offers Greenberger in view of Ganapathy and Sakai with respect to

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claims 1, 3, and 5-9, and Greenberger in view of Ganapathy and Antanaitis with respect to claim 4.

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the Briefs¹ and Answer for the respective details.

¹ The Appeal Brief was filed February 19, 1998 (Paper No. 18). In response to the Examiner's Answer dated March 31, 1998 (Paper No. 19), a Reply Brief was filed June 1, 1998 (Paper No. 20), which was acknowledged and entered by the Examiner as indicated in the communication dated June 19, 1998 (Paper No. 21).

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OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the Examiner, and the evidence of obviousness relied upon by the Examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellant's arguments set forth in the Briefs along with the Examiner's rationale in support of the rejection and arguments in rebuttal set forth in the Examiner's Answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claims 1 and 3-9. Accordingly, we reverse.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the Examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S.

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1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion, or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the Examiner are an essential part of complying with the burden of presenting a prima facie case of

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obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24
USPQ2d

1443, 1444 (Fed. Cir. 1992).

With respect to independent claims 1 and 9, the Examiner, as the basis for the obviousness rejection, proposes to modify the integrated circuit testing system disclosure of Greenberger. According to the Examiner, Greenberger discloses several key features of the claimed invention but lacks an explicit disclosure of the selection between a system clock signal and a test clock signal for normal operation and test operation, respectively, as well as program instruction implementation of the independent selection of the system clock signal or test clock signal. To address these deficiencies, the Examiner turns to Ganapathy which describes a microprocessor circuit for permitting internal microprocessor clock speed to vary dependent on a software programmed register. In the Examiner's view (Answer, page 5):

It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the High-Speed integrated circuit tester as taught by **Greenberger** by implementing instructions which independently

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select clocks of different frequencies (e.g., a test clock or a system clock) because it would provide **Greenberger's** system with the enhanced capability of software selection of system and test clock speeds.

The Sakai reference is added to the Examiner's proposed combination to provide an asserted teaching of accessing an auxiliary circuit when executing a program instruction from a subset of programs " . . . because it would provide the system taught by **Greenberger & Ganapathy** with the ability to efficiently switch the clock to an arbitrary value as required [col. 7, lines 34-36]." (Id. at 6).

In response, Appellant asserts a failure by the Examiner to establish a prima facie case of obviousness since, even if combined in the manner suggested by the Examiner, the references " . . . are still deficient of any disclosure or suggestion of the claimed subject matter" (Brief, page 7). After careful review of the applied prior art references in light of the arguments of record, we are in agreement with Appellant's position as stated in the Briefs.

In our view, the Examiner has combined the general clock frequency selection features of Ganapathy with the circuit testing system of Greenberger in some vague manner without

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specifically describing how the teachings would be combined, nor how any such combination would satisfy the requirements of appealed independent claims 1 and 9. This does not persuade us that one of ordinary skill in the art having the references before her or him, and using her or his own knowledge of the art, would have been put in possession of the claimed subject matter. The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992).

We further agree with Appellant that even assuming, arguendo, that the modification of Greenberger suggested by the Examiner were made, the resultant combination would not satisfy the claimed requirements. Each of the appealed independent claims 1 and 9 sets forth specific criteria for the selection between the system clock signal and the test clock signal. In contrast, as asserted by Appellant (Brief, page 6), the Ganapathy reference, applied by the Examiner to address the claimed clock selection feature, discloses nothing

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more than the software programming of clock speed that permits a microprocessor to operate at a plurality of user selected frequencies. There is no indication on the record by the Examiner as to how the proposed combination of Greenberger and Ganapathy would meet the specifics of the language of the claims on appeal. In order for us to sustain the Examiner's rejection under 35 U.S.C. § 103, we would need to resort to speculation or unfounded assumptions or rationales to supply deficiencies in the factual basis of the rejection before us. In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968), reh'g denied, 390 U.S. 1000 (1968).

With respect to the Sakai reference, added by the Examiner to the proposed combination of Greenberger and Ganapathy, we find that Sakai's disclosure does not cure the deficiencies of Greenberger and Ganapathy discussed supra. Regardless of the merits of the Examiner's contention that Sakai provides a teaching of auxiliary circuit access only when executing a program instruction from an instruction subset, we find no disclosure of the specific clock selection criteria set forth in Appellant's claims. Similarly, our

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review of the disclosure of Antanaitis, applied to address the coprocessor feature of dependent claim 4, reveals nothing that would overcome the previously discussed innate deficiencies of Greenberger and Ganapathy.

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Accordingly, since we are of the opinion that the prior art applied by the Examiner does not support the obviousness rejection, we do not sustain the rejection of independent claim

1 and 9, nor of claims 3-8 dependent thereon. Therefore, the decision of the Examiner rejecting claims 1 and 3-9 under 35 U.S.C. § 103 is reversed.

REVERSED

JOSEPH F. RUGGIERO)	
Administrative Patent Judge)	
)	
)	
)	BOARD OF PATENT
LANCE LEONARD BARRY)	APPEALS AND
Administrative Patent Judge)	INTERFERENCES
)	
)	
STUART S. LEVY)	
Administrative Patent Judge)	

JFR:hh

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