

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board

Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RICHARD J. DURANTE,
RODNEY R. ROZMAN and MICKEY L. FANDRICH

Appeal No. 1999-0045
Application 08/688,235

ON BRIEF

Before THOMAS, KRASS, and BARRETT, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellants have appealed to the Board from the examiner's final rejection of claims 1-4, 8-11, 15-18 and 22-26, which constitute all the claims on appeal.

Representative independent claim 1 is reproduced below:

1. A method for reducing the power consumed by a micro controller in a flash memory device, comprising the steps of:

receiving a user command over a host bus and storing the user command in an operation queue;

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enabling an oscillator circuit if the user command specifies an operation on a flash cell array by the micro controller, the oscillator circuit generating a clock signal for clocking the micro controller;

disabling the oscillator circuit when the operation is complete if a subsequent user command is not being received over the host bus.

The following references are relied on by the examiner:

Kreifels et al. (Kreifels)	5,222,046	June 22, 1993
Wells et al. (Wells)	5,265,059	Nov. 23, 1993 (filing date May 10, 1991)
Fandrich (Fandrich '300)	5,333,300	July 26, 1994 (filing date Feb. 11, 1991)
Fandrich et al. (Fandrich '256)	5,353,256	Oct. 4, 1994 (filing date June 30, 1993)

Applicant's admitted prior art, specification p. 2, lines 4-9.

All claims on appeal, claims 1-4, 8-11, 15-18 and 22-26 stand rejected under 35 U.S.C. § 103. In a first stated rejection, the examiner rejects claims 1-4, 8-11 and 22 in light of the collective teachings and showings of Fandrich '256 and Fandrich '300. These same claims stand rejected in a second stated rejection in light of Fandrich '256 in view of appellants' admitted prior art at page 2 of the specification as filed, lines 4-9. In a third stated rejection, the examiner rejects dependent claim 23 in light of Fandrich '256 in view of Fandrich '300, further in view of Wells. In a fourth stated rejection, the examiner rejects claim 23 in light of Fandrich '256 in view of the earlier noted portion of the specification at

page 2 identified as appellant's admitted prior art, further in view of Wells. For the fifth stated rejection, the examiner rejects claims 1, 2, 8, 9 and 22 in light of the collective teachings and showings of Kreifels in view of Fandrich '300. The examiner extends this rejection in a sixth stated rejection of claims 15, 16 and 23, further in view of Wells. Finally, in the seventh stated rejection, the examiner rejects claims 16-18 and 24-26 in light of Kreifels in view of Fandrich '300, further in view of Wells and Fandrich '256.

Rather than repeat the positions of the appellants and the examiner, reference is made to the brief and answer for the respective details thereof.

OPINION

For the reasons set forth by the examiner in the answer as amplified here, we sustain each of the seven stated rejections of all claims on appeal. From our study of appellants' arguments with respect to the first, second, fifth and sixth stated rejections as noted below, appellants have not argued against the combinability of the respective references relied upon by the examiner and appellants have also not argued the respective features of each of the independent claims in each of these noted rejections. However, appellants have argued the substance of what they consider a dispositive claimed feature of each of these stated rejections, that being the disablement of the oscillator circuit when the operation is complete if a subsequent user command is not being received over the host bus. Finally, because appellants have not directed any arguments to any of the

dependent claims within any of the above-stated rejections, including the separately stated rejections of claim 23 identified as rejections 3 and 4 below and the rejection of claims 16-18 and 24-26, identified as the seventh rejection, we sustain the rejection of each of these claims as well.

At the outset, we note that each of the respective four references relied upon by the examiner are variations upon prior art flash memory systems of the same assignee of the present application. The examiner asserts for each of the stated rejections 1, 2, 5 and 6 argued by appellants that it would have been obvious for the artisan to have improved upon the flash memory device of the base reference in light of the secondary and tertiary references. We agree. Since appellants have not contested this combinability, we agree with the examiner's reasoning for it particularly in light of the examiner's additional embellishments provided for all rejections at pages 19-21 of the answer.

Turning to the first stated rejection relying upon Fandrich '256, we note that this reference does not contain any particular teachings or showings of an oscillator or synch circuit within or related to the interface circuit 40 in Figures 3 and 4a of this reference. We embellish upon the examiner's reasoning by noting at the bottom of column 8 beginning at line 58 that the flash memory device of Fandrich '256 may be commanded to enter a shutdown operation to enter into a standby mode for reducing power consumption to the extent broadly recited in the preamble of each independent claim on appeal.

Correspondingly, Fandrich '300 has significant teachings of powering up and powering

down the so-called write state machine 48 in Figure 1 of this reference to effect power saving operations. This amounts to another reason for combinability in addition to that provided by the examiner. The examiner asserts, and we agree, that Fandrich '300 essentially teaches the subject matter of the last clause noted earlier with respect to representative independent claim 1 on appeal, a feature present in each independent claim on appeal.

Appellants' arguments with respect to the first stated rejection at pages 6-8 of the brief are unpersuasive of patentability. The claimed commands in both references relied upon in the first stated rejection relate to commands to program or erase data in the flash memory itself. The timing circuitry 42 in Figure 1 of the flash memory device of Fandrich '300 is detailed more particularly in Figure 3 and subsequent figures. As revealed in the discussion in the paragraph bridging columns 3 and 4, it is stated at lines 8-12 of column 4 that “[t]iming circuitry 42 also clearly powers up a clock associated with write state machine 48 and powers down the write state machine and its clock automatically upon completion of programming or erasure.” To the extent recited in each of the claims on appeal this directly relates to the enablement and disablement of the respective clock or oscillator circuits of each of the independent claims on appeal. This is more specifically recited at the bottom of column 5 where it is stated at lines 53 and 54 that the “automatic powering down of the WSM [write state machine] 48 cleanly shuts down the WSM

oscillator.” By implication then, the corresponding powering up operation would therefore power up or enable the WSM oscillator.

The above-quoted portion of column 4 indicates that the clock is disabled during the powering down operation “upon completion of programming or erasure.” Obviously, within 35 U.S.C. § 103, the artisan would have recognized that no power down operation would have occurred unless completion of programming or erasure operations would have occurred. Correspondingly, the disabling operations of the oscillator circuit are stated at the end of representative claim 1 on appeal to occur when the operation, that is, a command operation, is complete. This is consistent with the language quoted above from column 4. These features are further developed in the entire discussion of column 5 as well. However, the claim goes on to indicate that the disablement of the oscillator occurs when the operation is complete “if a subsequent user command is not being received over the host bus.” By implication, and the claims require, there will be no disablement operation of the oscillator if subsequent user commands are received over the host bus. Obviously, the system would not be permitted to shut down if more work was needed to be done. All this in fact is only common sense in the art anyway as well as reasonably taught and suggested to the artisan according to the earlier noted teachings in Fandrich '300.

The examiner's responsive arguments portion of the answer at page 15 as to this first stated rejection again brings in the basic teaching of Fandrich '256 concerning the existence of a queue for storing addresses and data that have been received by the flash

memory chip device in figure 3, the interface circuit of which is described in Figure 4a which includes a data/address queue 212 and an operation queue 214, both of which are fed by host bus 306. In the context of the overall discussion of Fandrich '300, the existence of any remaining commands to program and/or erase within the operation queue 214 obviously would not have permitted the disablement of the oscillator circuit according to the powering down operations identified earlier in that reference. The data including the command structure to program and/or erase operations are fed from the common bus 306 from the host processor itself according to the earlier Figures 1 and 2 of Fandrich '256. The conveyance of the commands from the microprocessor 999 at the bottom of Figure 1 of Fandrich '300 is stated there to be fed to the command state machine 40 and the write state machine 48 according to the address and data buses 20 and 21 and the control commands on buses 22-26, which obviously compare to the entire bus structure 306 Figure 1 of Fandrich '256 as well as its host bus 340 in the Figure 2 embodiment.

Turning to the second stated rejection, this rejection relies upon appellants' admitted prior art at the top of page 2 of the specification as filed, portions of which have been quoted at page 9 of the brief. As background to these statements, it is noted that the admitted prior art discussion at the bottom half of page 1 of the specification as filed indicates that user commands to prior art flash memory devices included commands for programming and erasing operations (both transferred over a host bus (specification, page 2, lines 12-13)) which utilized within the memory device itself specialized micro

controllers for performing these operations on the flash cell arrays per se. It is further stated there that these micro controllers were typically “driven” by the oscillator circuit associated therewith, which is further stated in the sentence bridging pages 1 and 2 to synchronize the operation of the micro controller. The statement in the admitted prior art portion of the specification at the top of page 2 relied upon the examiner indicates that the oscillator circuit is disabled after the micro controller executes a user command and shuts down. This is consistent with the disablement operation of the oscillator circuit when the operation is complete at the end of claim 1 on appeal. This disablement of the oscillator is said to halt the micro controller and reduce power consumption in accordance with the preamble of representative independent claim 1 on appeal. Lines 7 and 8 of this portion of page 2 of the specification indicates that the “oscillator circuit is then re-enabled when a subsequent user command is received.” This says nothing more than the fact that the oscillator circuit is not re-enabled or not enabled if a subsequent user command is not received. This is more consistent with the actual language of the entire disablement clause at the end of representative claim 1 on appeal. Again, as reasoned earlier with respect to the first stated rejection, this is only common sense in the art to the extent the artisan would fully appreciate operationally the functional sense, to the extent broadly recited, at the end of representative claim 1 on appeal based on the stated functionality of the admitted prior art.

In light of this we are unpersuaded of appellants' arguments as to this rejection at pages 8-10 of the brief. Appellants' statement at the middle of page 9 of the brief that “the admitted prior art will disable an oscillator circuit if a subsequent user command is being received over a host bus” is clearly misplaced or plainly wrong. The examiner emphasizes this at the top of page 17 of the answer. In any event, we read the functional operation of the admitted prior art discussed at specification page 2, lines 2-9 as relied upon by the examiner in the same manner as we read the specific teachings of Fandrich '300 in the first stated rejection.

We also do not agree with appellants' views expressed at pages 10 and 11 of the brief relative to the fifth stated rejection. These amount to only general arguments of patentability basically bottomed upon broad assertions not specifically developed. The examiner in the statement of the rejection according to this fifth stated rejection admits that Kreifels does not teach the disablement feature of representative claim 1 on appeal. Our discussion earlier in this opinion indicates our disagreement with appellants' view that Fandrich '300 does not teach the corresponding feature at the end of representative claim 1 on appeal argued in a general manner here.

Finally, we address appellants' arguments directed to the sixth stated rejection at pages 11-13 and find ourselves in agreement with the examiner's view as to the unpatentability of independent claim 15, its dependent claim 16 and dependent claim 23. The examiner's rejection relies upon Kreifels in view of Fandrich '300, further in view of

Wells as to this rejection. The examiner relies upon Wells to provide the synchronizer circuit of Figure 3 to provide the basis of the synchronizer of independent claim 15 according to the combination of references relied upon by the examiner. We agree with the examiner's view of Wells to the extent relied upon, but emphasize that the timing circuitry 42 of Figure 1 of Fandrich '300 is further shown in Figure 3 of this reference to contain the power up/down circuitry 50, handshaking circuitry 54 and synchronizing circuitry 52, each of which have been further developed in their own respective later disclosed figures in this reference. The stated function in independent claim 15 of the synchronizer circuit is to enable the oscillator and disable the oscillator, the functions of which we have already found in our earlier assessment of Fandrich '300 to include both stated functions of enabling and disabling the oscillator.

Appellants' arguments with respect to the sixth and last stated rejection at pages 11-13 of the brief are unpersuasive since they rely upon an assessment of the references relied upon which we do not agree with, principally appellants' view that Fandrich '300 does not teach the synchronizer circuit claimed, and as further developed according to the synchronizer circuit 30 in Figure 3 of Wells which feeds reset circuitry operations to the oscillator and as to the write state machine 32 in Figure 3 of Wells, the details of which are further developed in Figure 4 of this reference.

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In view of the foregoing, we have sustained each of the seven stated rejections of all the claims on appeal under 35 U.S.C. § 103. As such, the decision of the examiner rejecting all claims on appeal under 35 U.S.C. § 103 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

James D. Thomas)	
Administrative Patent Judge)	
)	
)	
)	BOARD OF PATENT
Errol A. Krass)	
Administrative Patent Judge)	APPEALS AND
)	
)	INTERFERENCES
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