

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHUEN-DER LIEN

Appeal No. 1998-2896
Application No. 08/558,564

ON BRIEF

Before HAIRSTON, GROSS, and BLANKENSHIP, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 30 through 37, 40 and 41.

The disclosed invention relates to a method of forming polycide over a semiconductor structure with an irregular upper surface. The polycide is used to form the gate electrodes of field effect transistors.

Appeal No. 1998-2896
Application No. 08/558,564

Appeal No. 1998-2896
Application No. 08/558,564

Claim 30 is illustrative of the claimed invention, and it reads as follows:

30. A method for forming polycide over a semiconductor structure having an irregular upper surface, the method comprising the steps of:

forming a first layer of non-monocrystalline silicon over the irregular upper surface of the semiconductor structure;

non- forming a dielectric layer over the first layer of monocrystalline silicon;

planarizing the first layer of non-monocrystalline silicon and the dielectric layer so as to provide the first layer of non-monocrystalline silicon and the dielectric layer with a substantially planar upper surface;

forming a second layer of non-monocrystalline silicon over the planar upper surface of the first layer of non-monocrystalline silicon and the dielectric layer; and

forming a layer of metal silicide over the second layer of non-monocrystalline silicon, wherein the dielectric layer separates portions of the first and second layers of non-monocrystalline silicon after the layer of metal silicide is formed.

The references relied on by the examiner are:

Tamura	4,900,690	Feb. 13, 1990
Hillenius et al. (Hillenius)	4,935,376	Jun. 19, 1990
Saitoh	5,332,692	Jul. 26, 1994

Wolf, "Silicon Processing For The VLSI Era," Volume 1: Process Technology, 175-82 (Sunset Beach, CA, Lattice Press, 1986).

Appeal No. 1998-2896
Application No. 08/558,564

Wolf, "Silicon Processing For The VLSI Era," Volume 2: Process Integration, 222-39 (Sunset Beach, CA, Lattice Press, 1990).

Appeal No. 1998-2896
Application No. 08/558,564

Claims 30, 32 and 40 stand rejected under 35 U.S.C. § 103 as being unpatentable over Tamura in view of Saitoh.

Claims 31 and 33 through 36 stand rejected under 35 U.S.C.

§ 103 as being unpatentable over Tamura in view of Saitoh, Hillenius and Wolf (Volume 2).

Claims 37 and 41 stand rejected under 35 U.S.C. § 103 as being unpatentable over Tamura in view of Saitoh and Wolf (Volume 1).

Reference is made to the briefs and the answer for the respective positions of the appellant and the examiner.

OPINION

The obviousness rejection of claims 30 through 37, 40 and 41 is reversed.

Tamura discloses a MOS semiconductor device (Figure 4D) with a silicon substrate 31, field oxide 32, gate oxide 35, polycrystalline silicon layer 36, insulating layer 38 and silicide layer 39. The insulating layer 38 is located between the polycrystalline silicon layer 36 and the silicide layer 39 in an area of the MOS device where the polycrystalline silicon layer 36 and the silicide layer 39 are not in direct contact.

Appeal No. 1998-2896
Application No. 08/558,564

The examiner acknowledges (Answer, page 4) that "Tamura lacks the teaching of the second non-monocrystalline [polycrystalline] silicon and thus the showing of the dielectric layer separating the polysilicon layers as now claimed [in claim] 38 but does show however the dielectric 38 separating portions of the polysilicon 36 with layers that are subsequently formed."

For a teaching of a semiconductor device with a plurality of polycrystalline silicon layers, the examiner turned to Saitoh. According to the examiner (Answer, pages 4 and 5), "Saitoh teaches forming on first polysilicon 3 having oxide film 4 thereon second polysilicon 7 and silicide 5, wherein the use of the second silicon obviates the need for cleaning the surface of the first polysilicon prior to forming the silicide and wherein the second polysilicon and the silicide are not separated from each other at their boundary interface." Based upon the teachings of Saitoh, the examiner concludes (Answer, page 5) that "[i]t would have been obvious to one skilled in the art at the time the invention was made in practicing the Tamura process to have employed the second polysilicon layer

Appeal No. 1998-2896
Application No. 08/558,564

on the first polysilicon layer in conjunction with the silicide layer as taught by Saitoh because such processing would obviate the need for cleaning the surface of the first polysilicon and would enable the formation of the silicide on a polysilicon without separation at their interface."

In Saitoh, a sputtering technique was used to place the second polycrystalline silicon film 7 over the first polycrystalline silicon film 3 and the natural oxide 4 located thereon (column 3, line 59 through column 4, line 3). The same sputtering technique was thereafter used to deposit the metal silicide film 5 over the second polycrystalline silicon film

7 (column 4, lines 4 through 29). The second polycrystalline silicon film 7 is used by Saitoh to bury the natural oxide 4 as opposed to removing the natural oxide by a problem-prone sputter etching technique (column 1, lines 27 through 51). According to Saitoh (column 1, lines 51 through 53), "[d]uring the sputter etching, a great quantity of particles are produced, which causes deterioration in product yield rate."

Notwithstanding the total lack of a need by Tamura to "clean" the surface of the polycrystalline silicon layer

Appeal No. 1998-2896
Application No. 08/558,564

36 (Brief, pages 11 and 12), the examiner proposes to subject it to Saitoh's cleaning process. In view of the total lack of a need for such a cleaning step in Tamura, we can only assume that the examiner wants to interject one in Tamura in order to meet the claimed limitation of "forming a second layer of non-monocrystalline silicon over the planar upper surface of the first layer of non-monocrystalline silicon." In short, the obviousness rejection of claims 30, 32 and 40 is reversed because we agree with appellant (Brief, page 12) that "there is no motivation to apply the cleaning steps taught by Saitoh to the Tamura process," and that "the Examiner has impermissibly used Applicant's specification as a template to piece together the teachings of Tamura and Saitoh."

The obviousness rejection of claims 31, 33 through 37 and 41 is reversed because Hillenius and the Wolf publications neither teach nor would have suggested the noted missing step in the teachings of Tamura.

Appeal No. 1998-2896
Application No. 08/558,564

DECISION

The decision of the examiner rejecting claims 30 through 37, 40 and 41 under 35 U.S.C. § 103 is reversed.

REVERSED

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KENNETH W. HAIRSTON))
Administrative Patent Judge)	
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)	BOARD OF PATENT
ANITA PELLMAN GROSS))
Administrative Patent Judge)	APPEALS AND
)	
)	INTERFERENCES
)	
HOWARD B. BLANKENSHIP)	
Administrative Patent Judge)	

KWH:hh

Appeal No. 1998-2896
Application No. 08/558,564

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