

The opinion in support of the decision being entered today was not written for publication is not binding precedent of the Board.

Paper No. 14

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KIN S. CHAN,
HUNG QUI LE and
DUNG Q. NGUYEN

Appeal No. 1998-2661
Application 08/633,267

ON BRIEF

Before THOMAS, FLEMING and HECKER, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellants have appealed to the Board from the examiner's final rejection of claims 1 through 16, 18 and 19. The examiner has allowed claim 20 and has objected to claim 17 as being

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dependent upon a rejected base claim, but further indicating it would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Representative claim 1 is reproduced below:

1. A processor comprising:

a set of N physical rename registers; and

circuitry for pre-assigning one of said N physical rename registers to an instruction before said one of said N physical rename registers is available to receive a result of said instruction.

The following references are relied upon by the examiner:

Sato	5,261,062	
Nov. 9, 1993		
Kau et al. (Kau)	5,491,829	Feb. 13,
1996		
Deosaran et al. (Deosaran)	5,590,295	Dec. 31,
1996		
		(filed June 7,
1995)		

Claims 1, 2, 13 and 16 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Kau. The examiner has extended the teachings and suggestions of Kau to reject claims 3 through 7 under 35 U.S.C. § 103. Finally, the examiner rejects all claims on appeal, claims 1 through 16, 18 and 19 under 35 U.S.C. § 103. As evidence of obviousness, the

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examiner relies upon Sato and in view of Deosaran.

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Rather than repeat the positions of the appellants and the examiner, reference is made to the brief and reply brief for appellants' positions, and to the first Office action, Paper No. 3, mailed on March 19, 1997, for statements of the rejections of the claims along with the examiner's responsive arguments in the answer.

OPINION

Turning first to the rejection of claims 1, 2, 13 and 16 under 35 U.S.C. § 102 as being anticipated by Kau, we reverse this rejection. The examiner's position is made clear in the positions set forth at pages 4 and 5 of the answer. These include the view that Kau's general purpose registers 62 correspond in an equivalent usage sense to the functioning of the claimed physical rename registers and that Kau's intermediate storage buffers 60 correspond to the claimed virtual rename buffers.

We basically agree with the appellants' view expressed primarily in the reply brief that the artisan would not have realized such a correspondence as argued by the examiner. We note also that claim 1 does not recite any virtual registers at all, only independent claim 13. Both claims do, however,

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recite the claimed physical rename registers. Appellants' background information provided at pages 1 through 3 of the specification as filed indicates that the so-called rename registers store instruction results prior to their commitment to the architected registers. The specification also indicates at lines 15 and 16 of page 8 that the concept of register renaming was well-known in the art and such registers were considered to be temporary storage registers. The notion of the use of the rename registers for temporary storage is also conveyed to the artisan at pages 8-9 and 8-10 of the PowerPC603 manual attached to the reply brief. Additionally, the discussion of rename registers at column 2, lines 29 through 55 of Kau itself confirms this functional usage.

The examiner's views as to the teaching value of Kau itself is not consistent with this view normally taken by the artisan. In the context of Kau's teachings and the examiner reliance upon Figure 3, it is the intermediate storage buffers 60 that perform the function of an intermediate storage comparable to the rename registers of the claims on appeal rather than the general purpose registers 62 as asserted by

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the examiner. In fact, the general purpose registers 62 of Kau perform a comparable function to the admitted prior art architected registers for final storage of the results of instruction execution as indicated in the background portion of appellants' specification. Therefore, the artisan would not have considered the examiner's views as indicating an anticipation of the noted claims within 35 U.S.C. § 102. In other words, according to the examiner's reasoning, the artisan would not have been placed into the possession of the claimed invention based upon the examiner's views as to Kau.

In light these findings, we cannot sustain the examiner's basis of the rejection of independent claims 1 and 13 and their respective dependent claims rejected, claims 2 and 16 under 35 U.S.C. § 102. For similar reasons, we must also reverse the rejection of dependent claims 3 through 7 under 35 U.S.C. § 103 over Kau alone.

On the other hand, we institute a new rejection of claims 1 through 3, 8, 12 through 16, 18 and 19 under 35 U.S.C. § 103 in light of the admitted prior art teachings of appellants at pages 2 and 3 of the specification as filed, further in view

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of Kau's teachings of prior art rename registers at column 2,
lines 29 through 55.

Kau teaches at column 2, lines 32 through 36 that
"[r]egister renaming is a technique utilized to temporarily
place the results of a particular instruction into a register
for

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potential use by later instructions prior to the time the final result from an instruction is placed within a register file." Kau's assessment of the prior art renders claim 1 obvious over Kau's prior art teachings by itself. This is essentially what is also stated by appellants' specification in the first paragraph at the top of page 3.

As to claim 2, the noted lines 29 through 55 of column 2 form a long paragraph which discusses in-part the use of table lookups and pointer systems in the context of register renaming systems of the prior art. Additionally, such pointer arrangements are stated to identify "particular physical registers which have been assigned to logical registers." The use of the terminology "logical registers," from an artisan's perspective, clearly indicates that a virtual register assignment of the type set forth in independent claim 13 and dependent claim 3 was contemplated or was known in the art. Furthermore, as to the details of claim 2, the use of such a logical register known in the art, as identified by Kau, would have further indicated to the artisan that consistent with classical computer architecture definitions of the word "virtual," in the context of storage systems, this terminology

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always has meant to connote that the execution unit effectively "sees" a larger storage space than is physically actually available for use. Hence, the artisan would have clearly realized from Kau's prior art logical registers that the number of virtual rename buffers of claim 2 would have been larger in number than the actual physical rename registers.

The discussion of pointers and lookup tables in the above-noted paragraph at column 2 of Kau renders obvious the subject matter of claim 3 on appeal.

As to claim 8, appellants' admitted prior art at pages 2 and 3 indicate that architected registers are known in the art to be used with rename registers. Claim 8 does not define the number of architected registers with respect to the number of physical rename registers or the number of logical or virtual registers. As to claim 12, both Kau and appellants' admitted prior art indicate that plural execution units are known to be a part of superscaler computer systems.

Turning to method independent claim 13, we apply this new rejection for the reasoning set forth with respect to claims 1 through 3, 8 and 12. Claim 13 is broader in one respect than

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claim 1 in that it recites that the assignment operation occurs "whether or not" the physical rename registers are available. This alternative construction not only reads upon the unavailability features as already indicated to be known in the art, but also when the registers are available. Obviously, within 35 U.S.C. § 103 in the context of claims 1 and 13, an instruction that has not yet been executed does not have any result that can be availably placed in any result register.

The subject matter of dependent claim 14 is a slightly more specific functional sequence than claim 13 implies and is considered inherent in the operation of the circuits of the admitted prior art and Kau. Appellants' admitted prior art clearly teaches the feature of dependent claim 15. As to dependent claim 16, because both Kau and appellants' admitted prior art relate to superscaler computer systems, a second or sequential instruction is specifically known to exist in these systems. In effect, the subject matter of claim 16 mimics the subject matter of independent claim 13 for a second labelled instruction.

As to claim 18, the rejection of this claim is consistent

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with our reasoning advanced earlier with respect to dependent claim 2. Finally, as to dependent claim 19, the subject matter of this claim is taught in appellants' admitted prior art at pages 2 and 3 of the specification as filed.

Before we leave our discussion of Kau, because independent claim 1 does not recite any feature relating to virtual rename buffers, the contribution of Kau per se also reads on the claimed subject matter because of the correspondence we indicated earlier. This includes our view that the intermediate storage buffers 60 of Figure 3 of Kau correspond to the claimed physical rename registers of this claim.

We disagree with appellants' view expressed at page 7 as to claim 1 that even if one were to make analogous the view of equating the recited physical rename registers of claim 1 with the storage buffers 60 taught in Kau, the reference teaches away because appellants take the view that Kau only assigns a storage buffer 60 to an instruction from an instruction dispatcher 22 when the storage buffer is available to receive a result. We do not read the Abstract, the Summary of the invention and the discussion of the operation of Kau's system between columns 5 through 7 in the manner urged by appellants. Indeed, it is clear that a pre-assignment occurs before the result of an given instruction is finally received in the intermediate and

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general purpose registers in this reference. Indeed, both alternative uses of the buffer index 58 shown in Figures 4 and 5 and discussed at column 7 clearly indicate that the corresponding relationship between the intermediate storage buffers and the general purpose registers is done before the result of a given instruction is obtained.

Kau is clearly in the same field of invention as appellants' disclosed and claimed invention because this reference deals with superscaler computer structure as indicated earlier. Indeed, both also are concerned with instruction execution and sequencing operations of an instruction dispatcher and any bottlenecks associated therewith. Because the intermediate storage buffers perform a temporary storage operation analogous to the traditional understanding the artisan has of physical rename registers, the artisan would have clearly considered the teachings to be analogous art within 35 U.S.C. § 103, appellants' arguments in the brief and reply brief notwithstanding. Additionally, because Kau teaches both his specific approach as well as the recognition of the existence of prior art approaches utilizing physical rename registers, when the teachings are properly

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weighed within 35 U.S.C. § 103, the artisan would not have considered this reference to teach away from the claimed invention to the extent we relied upon it.

Finally, we turn to the examiner's last stated rejection of all claims on appeal, claims 1 through 16, 18 and 19 as being obvious over the collective teachings and showings of Sato and Deosaran. We sustain this rejection only as to claim 1.

It appears that the examiner relies upon Sato only for those claims that specifically recite virtual rename buffers, and these include all claims on appeal except for claim 1. The examiner apparently sees some correspondence between the virtual registers associated with the pseudo-codes associated with source program instructions during a compiling operation and their relationship to corresponding real registers associated with finally converted machine codes. However, we are in agreement with appellants' views expressed at page 15 of the principal brief on appeal:

Sato is not relevant prior art to the present invention, since Sato teaches a process implemented within a compiler, and does not address the actual execution of instructions in parallel pipelines. As can be seen by noting Figure 3, step S10 converts the pseudo-code into

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machine codes at the end of the compiling process discussed in Sato. Sato never gets to the point of addressing what occurs during execution of the instructions. Sato is not reasonably pertinent to the particular problem with which the invention were concerned, since Sato pertains to the compiling of pseudo-code into machine code prior to any execution of instructions, while the inventors were concerned with the actual execution of instructions, and were not concerned with the compiling of pseudo-code.

Not only do we agree with appellants' view as to Sato as just expressed in this quoted portion of the brief, we see no relevance of Sato to Deosaran for combinability purpose within 35 U.S.C. § 103. Deosaran's invention is a system and method for register renaming (see the title). His invention is directed to superscaler operations in the same manner as disclosed with respect to appellants' invention. Not only do we agree with appellants' view that Sato is not analogous art to the presently claimed invention, it appears to be nonanalogous to the subject matter of Deosaran. Our study of both references leads us to conclude that the artisan would not have seen any relevance of the virtual registers of Sato in a compiling operation to the register renaming operations of Deosaran in actual instruction sequencing operations during their execution. We conclude that the artisan would not have

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found it obvious to therefore combine the teachings and suggestions of the two references together as urged by the examiner.

Since Sato is the only reference relied upon by the examiner in this rejection which provides a basis for the claimed virtual rename buffers, we are left with no reference which teaches or relates to virtual rename buffers in an instruction execution environment as recited in claims 2 through 16, 18 and 19. Therefore, we reverse the rejection of these claims in light of the examiner's combination of Sato and Deosaran.

On the other hand, we sustain the rejection of independent claims 1 over Deosaran alone. We do not agree with appellants' urgings in the brief that Deosaran does not teach the pre-assignment of physical rename registers to an instruction before the register is available to receive the result of the execution of that instruction. Deosaran's register renaming circuit RRC in-part makes use of a variable advance instruction window VAIW. Within Deosaran the renaming function occurs when a new instruction enters this window. So-called tags are assigned

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to the instructions as they enter this VAIW as expressed in the discussion between columns 3 through 5 of Deosaran and most succinctly expressed at the bottom of column 3 at lines 59 through 62 "[e]ach instruction's tag remains constant as long as the instruction remains in the window. This tag is also associated with the location in a temp buffer (discussed below) that the corresponding instruction's output will be stored."

From an artisan's perspective, this temporary buffer is clearly analogous to the claimed physical rename registers in a manner well-expressed earlier in this opinion in terms of their functionality. Thus, it is apparent that this temporary buffer is reassigned according to the tagging scheme and associated with an instruction before the availability of the buffer to receive the result of that instruction in accordance with that which is set forth in claim 1 on appeal. This pre-assignment is necessary and indirectly expressed again at column 5, lines 29 through 32 indicating "the processor implementing the present invention uses the tag of an instruction as the temp buffer address of that instruction's result." Therefore, we only sustain the rejection of claim 1

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as part of that rejection the examiner has set forth relying upon the combination of Sato in view of Deosaran.

In summary, we have reversed the rejection of claims 1, 2, 13 and 16 under 35 U.S.C. § 102 as being anticipated by Kau and the rejection under 35 U.S.C. § 103 of claims 3 through 7 over this reference. We have also reversed the rejection of claims 2 through 16, 18 and 19 under 35 U.S.C. § 103 in light of the collective teachings and showings of Sato and Deosaran, but have sustained only the rejection of claim 1 on this combination of references. We have also instituted a new ground of rejection under 35 U.S.C. § 103 over appellants' admitted prior art in view of Kau as to claims 1 through 3, 8, 12 through 16, 18 and 19.

In addition to affirming the examiner's rejection of one or more claims, this decision contains a new ground of rejection pursuant to 37 C.F.R. § 1.196(b) (amended effective Dec. 1, 1997, by final rule notice, 62 Fed. Reg. 53,131, 53,197 (Oct. 10, 1997), 1203 Off. Gaz. Pat. & Trademark Office 63, 122 (Oct. 21, 1997)). 37 C.F.R. § 1.196(b) provides, "A new ground of rejection shall not be considered final for purposes of judicial review."

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Regarding any affirmed rejection, 37 C.F.R. § 1.197(b) provides:

(b) Appellant may file a single request for rehearing within two months from the date of the original decision

37 C.F.R. § 1.196(b) also provides that the appellants, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of proceedings (37 C.F.R. § 1.197(c)) as to the rejected claims:

(1) Submit an appropriate amendment of the claims so rejected or a showing of facts relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the application will be remanded to the examiner. . . .

(2) Request that the application be reheard under § 1.197(b) by the Board of Patent Appeals and Interferences upon the same record. . . .

Should the appellants elect to prosecute further before the Primary Examiner pursuant to 37 C.F.R. § 1.196(b)(1), in order to preserve the right to seek review under 35 U.S.C. §§ 141 or 145 with respect to the affirmed rejection, the effective date of the affirmance is deferred until conclusion of the prosecution before the examiner unless, as a mere incident to the limited prosecution, the affirmed rejection is

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overcome.

If the appellants elect prosecution before the examiner and this does not result in allowance of the application, abandonment or a second appeal, this case should be returned to the Board of Patent Appeals and Interferences for final action on the affirmed rejection, including any timely request for rehearing thereof.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED-IN-PART
37 C.F.R. § 1.196(b)

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Administrative Patent Judge)	
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)	BOARD OF PATENT
MICHEAL R. FLEMING)	APPEALS
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