

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 42

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte KIM C. HARDEE

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Appeal No. 1998-1657  
Application No. 08/674,282

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ON BRIEF

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Before KRASS, BARRETT, and BARRY, Administrative Patent Judges.  
BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the rejection of claims 5-7, 20-26, and 28-39. We reverse.

BACKGROUND

The invention at issue in this appeal is a sense amplifier for use in an integrated circuit (IC) memory. An IC memory includes many memory cells, which are arranged in rows

and columns. A column is a collection of memory cells along a bit line pair. Each column is connected to a sense amplifier. The sense amplifier senses the effect a memory cell has on the bit line pair and amplifies a signal for reading data from the memory cell. In addition, the sense amplifier drives, i.e., controls, the bit line pair for writing data into the memory cell.

When conventional sense amplifiers are employed in large memories, the amplifiers work inefficiently and slowly, prolong access time, suffer pattern sensitivities, and are unstable. The invention aims to overcome these problems. In particular, the inventive sense amplifier includes a sense amplifier latch coupled to a pair of bit lines of an IC memory. A local column read amplifier is coupled to data read lines and to internal nodes of the latch.

Claim 35, which is representative for our purposes, follows:

35. A sense amplifier arrangement for an integrated circuit memory, the sense amplifier arrangement

corresponding to a bit line pair within the memory,  
the arrangement comprising:

a sense amplifier latch configured to develop  
voltages on a pair of latch nodes, said voltages  
corresponding to signals on said bit line pair in  
connection with a read operation;

first and second local sense amplifier drive  
transistors connected respectively to provide  
selectively first and second power supply voltages  
to said latch;

a local column read amplifier and a pair of data  
read lines coupled thereto,

said read amplifier including means responsively  
coupled to at least one of said latch nodes for  
developing a differential signal on said pair of  
data read lines, said differential signal being  
based on the state of at least one of said latch  
nodes.

The references relied on in rejecting the claims follow:

U.S. Patent Application 08/684,328 ('328  
Application) (filed July 17, 1996)

U.S. Patent Application 08/284,183 ('183 Application)  
(filed Aug. 2, 1994)

Young 5,247,479 Sep. 21, 1993  
(filed May 23, 1991)

Toshiba et al. (Toshiba), European Patent  
Application 0 175 880 Apr. 2, 1986.

Claims 5-7, 20-26, and 28-39 stand provisionally rejected under the doctrine of obviousness-type double patenting as unpatentable over claims 13-46 of the '328 Application and over claims 8, 9, and 14-50 of the '183 Application. Claims 5-7, 20-26, and 28-39 also stand rejected under 35 U.S.C. § 103 as obvious over Young in view of Toshiba. Rather than repeat the arguments of the appellant or examiner in toto, we refer the reader to the briefs and answer for the respective details thereof.

#### OPINION

In reaching our decision in this appeal, we considered the subject matter on appeal and the rejection and evidence advanced by the examiner. Furthermore, we duly considered the arguments of the appellant and examiner. After considering the totality of the record, we are persuaded that the examiner erred in rejecting claims 5-7, 20-26, and 28-39. Accordingly, we reverse. Our opinion addresses the following rejections:

- obviousness-type double patenting
- obviousness.

We begin by addressing the rejections for obviousness-type double patenting.

Obviousness-Type Double Patenting

Regarding the obviousness-type double patenting rejection over claims 13-46 of the '328 Application, the appellant argues, "[c]laims 5-7, 20-26, and 28-39 ... are directed to a sense amplifier with a column read amplifier and local sense amplifier drive transistors, and are not directed to a method which is the subject of the related application." (Appeal Br. at 39.) Regarding the obviousness-type double patenting over claims 8, 9, and 14-50 of the '183 Application, the appellant argues, "[c]laims 5-7, 20-26, and 28-39 are not directed to an apparatus, that requires pass transistors nor local data write driver circuits and which is the subject of the related application." (Id. at 40.) The examiner collectively responds, "claims 5-7, 20-26 and 28-39 ... have been amended and changed since the original restriction requirement and hence are not consonant with the restriction requirement made by the Examiner ...." (Examiner's Answer at 8.)

We note the following principles concerning consonance from Symbol Technologies Inc. v. Opticon Inc., 935 F.2d 1569, 1579, 19 USPQ2d 1241, 1249 (Fed. Cir. 1991).

Consonance requires that the line of demarcation between the "independent and distinct inventions" that prompted the restriction requirement be maintained. Though the claims may be amended, they must not be so amended as to bring them back over the line imposed in the restriction requirement. Where that line is crossed the prohibition of the third sentence of Section 121 does not apply.

Gerber Garment Technology Inc. v. Lectra Systems Inc., 916 F.2d 683, 688, 16 USPQ2d 1436, 1440 (Fed. Cir. 1990). The corollary to this Court's statement in Gerber Garment is that new or amended claims in a divisional application are entitled to the benefit of § 121 if the claims do not cross the line of demarcation drawn around the invention elected in the restriction requirement.

With these principles in mind, we address the obviousness-type double patenting rejections over claims 13-46 of the '328 Application and over claims 8, 9, and 14-50 of the '183 Application separately.

*Obviousness-Type Double Patenting over the '328 Application*

The examiner fails to show a loss of consonance between claims 13-46 of the '328 Application and the claims of the instant application. In U.S. Patent Application 07/976,312 ('312 Application), the parent application of the instant application, the examiner issued a restriction requirement dividing the initial claims into five groups. (Paper No. 3 at 2.) He explained that the fifth group comprised "[c]laim 13, drawn to a method of operating a sense amplifier utilizing a read amplifier and data write circuitry ...." (Id.) It is uncontested that the appellant elected to prosecute claim 13

and claims similar thereto in the divisional '328 Application and its parent application. (Appeal Br. at 38.)

Although claims 5-7, 20-26, and 28-39 of the instant application have been amended since the restriction requirement, the examiner fails to allege, let alone show, that the claims have been altered to recite a method of operating a sense amplifier utilizing a read amplifier and data write circuitry or a method of any sort. To the contrary, the claims are still apparatus claims drawn to "[a] sense amplifier arrangement for an integrated circuit memory . . . ." Cf. Applied Mats., Inc. v. Advanced Semiconductor Mats., 98 F.3d 1563, 1568, 40 USPQ2d 1481, 1484 (Fed. Cir. 1996) ("In this case consonance was not violated, for the process claims remained in separate patents from the apparatus claims although the scope of the process claims was modified.") The claims also omit data write circuitry. Because claims 5-7, 20-26, and 28-39 recite neither a method nor data write circuitry, we are not persuaded that the claims cross the line of demarcation drawn in the restriction requirement. Therefore, we reverse the provisional rejection

of claims 5-7, 20-26, and 28-39 over claims 13-46 of the '328 Application.

*Obviousness-Type Double Patenting over the '183 Application*

The examiner fails to show a loss of consonance between claims 8, 9, and 14-50 of the '183 Application and the claims of the instant application. In the restriction requirement of the '312 Application, he explained that the third group comprised "[c]laims 8-9, drawn to a sense amplifier utilizing a data write driver circuit for write operation ...." (Paper No. 3 at 2.) It is uncontested that these are the claims in the '183 Application. (Appeal Br. at 40.)

Although claims 5-7, 20-26, and 28-39 have been amended since the restriction requirement, the examiner fails to allege, let alone show, that the claims have been altered to recite a sense amplifier utilizing a data write driver circuit for a write operation. To the contrary, the claims omit a data write driver circuit. The claims further omit a write operation. Because claims 5-7, 20-26, and 28-39 recite neither a data write driver circuit nor a write operation, we

are not persuaded that the claims cross the line of demarcation drawn in the restriction requirement. Therefore, we reverse the provisional rejection of claims 8, 9, and 14-50 of the '183 Application. We next address the rejection for obviousness.

#### Obviousness

We note the following principles from In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993).

In rejecting claims under 35 U.S.C. section 103, the examiner bears the initial burden of presenting a prima facie case of obviousness. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).... "A prima facie case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." In re Bell, 991 F.2d 781, 782, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting In re Rinehart, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)). If the examiner fails to establish a prima facie case, the rejection is improper and will be overturned. In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

With these principles in mind, we address the examiner's rejection and the appellants' argument.

The examiner's rejection follows in pertinent part.

Young shows all the limitations of the claimed sense amplifier arrangement in figs.1-4, comprising a sense amplifier latch circuit 21a-24b and a local column read amplifier 25,27,YDR,S, S, in each sense amplifier circuit, except the use of first and second local sense amplifier drive transistors, as recited in claims 5,25,33 and 35.

However, EP (`880) shows a plurality of sense amplifier 57 each comprising a latch circuit 51-56 and first and second local sense amplifier drive transistors 58 and 61 in figs 1-13.

(Final Rejection at 3.) The appellants argue, "21a-24b of Young form a memory cell latch and not a sense amplifier latch, and 25, 27, 28 form a column sense amplifier and not a sense amplifier latch." (Reply Br. at 5.) They further argue, "25, 27, 28 is a column sense amplifier, not a read amplifier." (Id. at 11.)

Claim 5-7 and 20-24 specify in pertinent part the following limitations:

a plurality of column read amplifiers  
corresponding to said plurality of sense amplifiers;  
and

a plurality of data read lines;  
each said column read amplifier being  
responsively coupled to at least one of said  
internal nodes of the latch circuit of the  
corresponding sense amplifier, each said column read  
amplifier being coupled to at least one said data  
read line.

Similarly, claim 25, 26, and 28-32 specify in pertinent part the following limitations:

a plurality of local column read amplifiers corresponding to said plurality of sense amplifiers; first and second data read lines,  
...  
each said local column read amplifier being connected to said first and second data read lines, each said local column read amplifier including a plurality of read amplifier transistors, at least one of said plurality of read amplifier transistors having a control electrode responsively coupled to one of said internal nodes of said latch ....

Also similarly, claim 33 and 34 specify in pertinent part the following limitations:

first and second data read lines;  
a local column read amplifier corresponding to said sense amplifier latch circuit, said local column read amplifier including a plurality of read amplifier transistors, said local column read amplifier being connected to said first and second data read lines, at least one of the plurality of read amplifier transistors in the local column read amplifier being responsively coupled to an internal node of said latch circuit ....

Further similarly, claim 35-39 specify in pertinent part the following limitations:

a local column read amplifier and a pair of data read lines coupled thereto,  
said read amplifier including means responsively coupled to at least one of said latch nodes for developing a differential signal on said pair of data read lines, said differential signal being

based on the state of at least one of said latch nodes.

Accordingly, the limitations of claims 5-7, 20-26, and 28-39 require a local column read amplifier coupled to data read lines and to an internal node of a sense amplifier latch.

The examiner fails to show a suggestion of the limitations in the prior art. "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." Para-Ordnance Mfg. v. SGS Importers Int'l, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995)(citing W.L. Gore & Assocs., Inc. v. Garlock, Inc., 721 F.2d 1540, 1551, 1553, 220 USPQ 303, 311, 312-13 (Fed. Cir. 1983)). "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992) (citing In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)).

The prior art belies the examiner's allegation that elements 21a, 21b, 24a, and 24b of Young form a sense amplifier latch while elements 25, 27, and 28 of the reference form a local column read amplifier. (Final Rejection at 3.)

"Every patent application and reference relies to some extent upon knowledge of persons skilled in the art to complement that [which is] disclosed ....'" In re Bode, 550 F.2d 656, 660, 193 USPQ 12, 16 (CCPA 1977) (quoting In re Wiggins, 488 F.2d 538, 543, 179 USPQ 421, 424 (CCPA 1973)). Those persons "must be presumed to know something" about the art "apart from what the references disclose." In re Jacoby, 309 F.2d 513, 516, 135 USPQ 317, 319 (CCPA 1962).

Here, U.S. Patent 5,265,047 (Leung), which the examiner "made of record" in the '213 Application, (Paper No. 16 at 5.), evidences that in memory circuits comprising memory cells and a sense amplifier, word lines are used by the memory cells rather than the sense amplifier. Specifically, "two separate word lines (WL and WLC) are used in each memory cell." Col. 3, ll. 54-54. Figure 3 of the reference specifically shows

that the word lines WL and WLC are connected to memory cells 400 and 500 rather than to sense amplifier 504.

Similarly, Figure 2a of Young shows word line WL connected to elements 21a, 21b, 24a, and 24b. As evidenced by Leung and contrary to the examiner's allegation, therefore, persons skilled in the art would interpret the elements as forming a memory latch rather than a sense amplifier latch. Also contrary to the examiner's allegation, such persons would then interpret elements 25, 27, and 28 as the "local or column sense amplifier," col. 1, ll. 65-66, shown in the Figure rather than as a local column read amplifier. In summary, the examiner fails to show that Young teaches a local column read amplifier let alone such an amplifier coupled to data read lines and to an internal node of a sense amplifier latch. He fails to allege, let alone show, that Toshiba remedies the defect of Young.

Because Young omits a local column read amplifier, we are not persuaded that teachings from the prior art would have suggested the limitations of "a plurality of column read

amplifiers ... each said column read amplifier being responsively coupled to at least one of said internal nodes of the latch circuit of the corresponding sense amplifier, each said column read amplifier being coupled to at least one said data read line"; "a plurality of local column read amplifiers ... each said local column read amplifier being connected to said first and second data read lines ... at least one of said plurality of read amplifier transistors having a control electrode responsively coupled to one of said internal nodes of said latch ..."; "a local column read amplifier ... said local column read amplifier including a plurality of read amplifier transistors, said local column read amplifier being connected to said first and second data read lines, at least one of the plurality of read amplifier transistors in the local column read amplifier being responsively coupled to an internal node of said latch circuit ..."; and "a local column read amplifier and a pair of data read lines coupled thereto ... said read amplifier including means responsively coupled to at least one of said latch nodes ...." The examiner fails to establish a prima facie case of obviousness. Therefore, we reverse the rejections of claims

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5-7, 20-26, and 28-39 as obvious over Young in view of  
Toshiba.

CONCLUSION

To summarize, the provisional rejections of claims 5-7, 20-26, and 28-39 under the doctrine of obviousness-type double patenting as being unpatentable over claims 13-46 of the '328 Application and over claims 8, 9, and 14-50 of the '183 Application are reversed. The rejection of claims 5-7, 20-26, and 28-39 under 35 U.S.C. § 103 as obvious over Young in view of Toshiba is also reversed.

REVERSED

|                             |   |                 |
|-----------------------------|---|-----------------|
| ERROL A. KRASS              | ) |                 |
| Administrative Patent Judge | ) |                 |
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|                             | ) |                 |
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|                             | ) | BOARD OF PATENT |
| LEE E. BARRETT              | ) | APPEALS         |
| Administrative Patent Judge | ) | AND             |
|                             | ) | INTERFERENCES   |
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| LANCE LEONARD BARRY         | ) |                 |
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