

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DANIEL R. EDWARDS, GEORGE E. REASONER, JR. and
GERALD R. SMITH

Appeal No. 98-1396
Application 08/300,666¹

ON BRIEF

Before JERRY SMITH, BARRETT and DIXON, **Administrative Patent Judges.**

DIXON, **Administrative Patent Judge.**

DECISION ON APPEAL

This is a decision on appeal from the Examiner's final rejection of claims 2, 7-10, 14, 15, 17, and 23-29, which are all of the claims pending in this application.

¹ Application for patent filed September 2, 1994.

BACKGROUND

The present invention relates to a method and apparatus for processing either single-bit or multi-bit images in a scaler/normalizer section of an image processing system. The invention may be used for processing black and white pixel data or gray scale data and scaling using both adjacent pixel and adjacent scan line methodologies. The invention is disclosed as using a combination of two ROMs, a current pixel ROM R-1 and a previous pixel ROM R-2, which may be programmed with any number and combination of scaling algorithms. The ROMs are programmed to include a table for each algorithm which maps actual input pixel values to new pixel values according to the stored algorithm which is embodied in the table. The use of the ROMs is disclosed to be faster since the values are precalculated, stored and addressed by the system. The system is also flexible due to the interchangeability of the ROMs for new or different algorithms.

Appellants have indicated that claims 2, 7-10, 14, 15, 17, and 23-26 do not stand or fall together. Appellants also indicate that claims 27-29 stand or fall with claim 26. (Brief at page 5.)

Independent claim 23 is representative of the invention and reproduced as follows:

23. An arrangement for extracting and processing single-bit or multi-bit image data to form an array of re-scaled pixel data, this arrangement being part of a Normalizer/Scaler stage in an image lift/processing system, and including:

flexible, variable scaler means for storing a number of different selectable [sic] scaling algorithms; scaler-output means; and input means for receiving scanned lines of pixel data and feeding it sequentially line-by-line, pixel-by-pixel to said scaler means; and input means also including "scale factors" for selecting a said algorithm; said scaler means including mapping means for executing a two-dimensional mapping of adjacent pixel values and adjacent scan line values; said arrangement also including command store means for storing said scaling algorithms with a command register input for said scale factors;

wherein said scaler means also includes a First ROM R-1 input by said input means for storing pixel values at prescribed addresses; a Second ROM R-2 for similarly storing previous pixel values, being input in parallel with First ROM R- 1; Latch means to which said ROMs are output; and pixel Count means reset with each new scan line;

wherein a "current pixel" value is input to a prescribed address in said First ROM, along with a "pixel count" number from said Count means, and an associated scale factor; and

wherein Adder means is interposed between said ROMs and said Latch means to execute addition mapping.

The prior art references of record relied upon by the Examiner in rejecting the appealed claims are:

Ohuchi	4,907,284	Mar. 06, 1990
Hackett et al.	5,140,648	Aug. 18, 1992

Claims 2, 7-10, 14, 15, 17, and 23-29 stand rejected under 35 U.S.C. § 103 as being unpatentable over Ohuchi in view of Hackett.

Claims 7-10 stand rejected under 35 U.S.C. § 112 first paragraph, as being based upon a lack of written description.

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Claims 2, 7-10, 14, 15 and 17 stand rejected under 35 U.S.C. § 112 second paragraph.

Rather than reiterate the conflicting viewpoints advanced by the Examiner and the appellants, we make reference to the appeal brief, filed July 28, 1997, (Paper No. 13) and examiner's answer mailed November 17, 1997, (Paper No. 14) and remailed on June 29, 1998, (Paper No. 16) for the details thereto.

OPINION

After a careful review of the evidence before us, we reverse.

As a consequence of our review, we make the determinations which follow.

OBJECTIONS

We are limited in our scope of review merely to consider rejections of claims based upon the administrative record. See **In re Hengehold**, 440 F.2d 1395, 169 USPQ 473 (CCPA 1971). Appellants have presented argument in the brief that the Examiner previously indicated claim 13 as allowable and that the new independent claims were drafted similar to claim 13. The Examiner has rebutted the argument

thereto. If appellants dispute the administrative processing of the prosecution, the proper procedure is to seek review by way of petition to the Commissioner/Group Director.

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Therefore, we make no findings thereto. Furthermore, the Examiner has included objections in the examiner's answer. The objection to the specification based on 35 U.S.C. § 112, first paragraph, lack of written description is an "objection" under 35 U.S.C. § 132, which the Board has no jurisdiction to review. Such matters are reviewable by petition to the Commissioner. The Board's jurisdiction is limited to those matters involving the rejection of claims. *Id.* 440 F.2d at 1404, 169 USPQ at 480. However, our decision regarding the § 112 rejection governs the merits of the objection.

35 U.S.C. § 112, FIRST PARAGRAPH

We address the rejections under 35 U.S.C. § 112, first and second paragraphs, for completeness rather than summarily sustain the rejections. Claims 7-10 are rejected under 35 U.S.C. § 112, first paragraph, based on lack of an adequate written description. The Examiner has only rejected claims 7-10.

The Examiner has set forth rejections under 35 U.S.C. § 112, first and second paragraphs, in the final Office action. Appellants responded in an after-final amendment. In response to the amendment after final filed March 28, 1997, (Paper No. 11), by appellants, the Examiner mailed an Advisory action on May 1, 1997, (Paper No. 12), indicating that the Examiner would enter the amendment upon filing an appeal and that the claims remained rejected. The Advisory action did not indicate that any rejections were

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overcome. Appellants did not address the rejections under 35 U.S.C. § 112, first and second paragraphs, in the brief and indicated in the brief that the copy of the advisory action received was not legible. If appellants desired a better copy, then a request to the Examiner should have been filed. The Examiner again included the same rejections in the Examiner's answer. Again, appellants did not address these rejections made in the answer and did not file a reply brief to address these issues.

Nevertheless, we have reviewed the specification as it relates to the claimed invention set forth in the chain of dependency of claims 7/24; 8/7/24; 9/8/7/24; 10/9/8/7/24 and we cannot sustain the rejections of the listed claims with regards to the issues (a)-(d) raised by the Examiner at page 3 of the final rejection and pages 4-5 of the answer.

With respect to issue (a), none of the rejected claims 7-10 recite "valid/invalid markers", therefore, there is no basis for the rejection in the language of the claims. We note that claims 27 and 14 contain these limitations, but were not rejected by the Examiner. We have reviewed the specification and find adequate support for

valid/invalid markers in the specification, as originally filed, at pages 17-20. Therefore, this reason for the § 112 rejection is reversed.

With respect to issue (b), "scale factors" are recited in claims 8 and 9 (and their

parent independent claim 24, which was not rejected). From a review of the specification at page 15, paragraph 3, page 16, paragraph 2, and the prior art, it is clear that the "scale factor" is disclosed to be an input to select the stored algorithm to be used in scaling the pixel data. Therefore, this reason for the § 112 rejection is reversed.

With respect to issue (c), the parallel input of the addresses to the ROMs, it is clear from a review of figure 1 and the supporting description in the specification that the purpose of the input of data in parallel to the ROMs is to have the stored data addressed simultaneously for output and subsequent processing by the adder and latch. The parallel input of the data to the ROMs would have been clear to skilled artisans with respect to proper operation thereof. Therefore, this reason for the § 112 rejection is reversed.

With respect to issue (d), "variable" and "flexible," we do not find these terms in the rejected claims or the parent independent claim 24. Therefore, there is no basis for the rejection in the language of the claims. We do find the claim language in

independent claims 23 and 25 which were not rejected by the Examiner. We find that these are merely asserted statements of advantages of the invention which would not be given patentable weight unless there is some structure in the language of the claim which provides for the functionality of the advantage. The disclosed functionality is provided by

the ROMs which are programmed to include a table for each algorithm to map actual input pixel values to new pixel values according to the stored algorithm which is embodied in the table. The use of the ROMs is disclosed to be faster since the values are precalculated and stored for subsequent addressing. The system is also flexible due to the interchangeability of the ROMs for new or different algorithms.

Accordingly, we will not sustain the Examiner's rejection of claims 7-10 under 35 U.S.C. § 112, paragraph one.

35 U.S.C. § 112, SECOND PARAGRAPH

Claims 2, 7-10, 14, 15 and 17 are rejected under 35 U.S.C. § 112, second paragraph. First, the rejection of claims 2, 7-10, 14, 15 and 17 is based upon dependence from a canceled parent claim. The rejection is moot in view of the entry of the after final amendment which corrected the erroneous dependencies. Second, the term "selectible [sic] scaling algorithms" in claim 7 is originally introduced in the rejected claim and therefore does not lack a proper antecedent basis as asserted by the

Examiner. Accordingly, we will not sustain the Examiner's rejection of claims 2, 7- 10, 14, 15 and 17 under 35 U.S.C. § 112, second paragraph.

35 U.S.C. § 103

Claims 2, 7-10, 14, 15, 17, and 23-29 are rejected under 35 U.S.C. § 103.

Appellants summarily argue by listing distinctions which paraphrase intended claim limitations which are purported to correspond to the claims. (See brief at pages 11-12). We do not find that appellants have provided a clear representation of the limitations as they appear in the varied claims before us for review.

We conclude that it would not have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Ohuchi with those of Hackett as asserted by the Examiner. The Examiner states that "it would have been obvious . . . to incorporate such specific circuitry in Ohuchi's system . . . as taught by Hackett et al." (See answer at page 7.) Ohuchi discloses a hardwired shrinking circuit where the ROM is not used in the scaling of the data. The ROM is used in the packing operation rather than the scaling of the data. Furthermore, Hackett does not specifically disclose the use of a ROM. Hackett teaches the storage of a value of the number of pixels in the data register B and storage of a number of pixels needed to complete a grouping in register A. (See Fig. 5.) These registers do not function in the same manner as the ROM in the claimed invention which has the new pixel data stored in the ROM at prescribed addresses and the current pixel is input to a prescribed address, to read out the new pixel value. Therefore, one of ordinary skill in the art of scaling images would not have been motivated by the register teachings of Hackett to modify Ohuchi to arrive at the

claimed ROMs. Moreover, the motivation set forth by the Examiner is merely a conclusion without supporting reasoning. (See Answer at page 7.)

Alternatively, assuming arguendo that the combination of references is proper, we find that the combination of references do not teach the common elements as set forth in the language of the independent claims. The Examiner has stated that "Ohuchi does not disclose the specific structure/design including a second ROM, a counter and a latch." (See Answer at page 6.) We do not find even a first ROM in Ohuchi which is "input by the input means for storing pixel values at prescribed addresses." (See claim 23, paragraph 3.) Ohuchi merely discloses the use of the ROM for the rotation and packing of the output data. (See col. 2, lines 29-30.) Furthermore, Ohuchi does not disclose the use of prior pixels by "a second ROM for similarly storing previous pixel values" nor the combination of the "[latch means to which the ROMs are output" and "wherein [adder means is interposed between the ROMs and said latch means to execute addition mapping." (see Claim 23.)

Hackett does not provide these missing teachings from Ohuchi. Regarding the correlation of Hackett to limitations in the claims, the Examiner has stated that "the scaler means also includes a first ROM input by [an] input means for storing pixel values at prescribed address (Figure 5:8); a second ROM for similarly storing previous pixel values

(Figure 5: A, note the previous pixel numbers being stored), being input in parallel with the first ROM (note the parallel input of Figure 5: B and A); match means to which the ROMs are output (Figure 6: 25 and 27)." (See Answer at page 6, paragraph 2.) From a review of Hackett, it is clear that Hackett discloses "registers" A and B which temporarily store data input thereto. (See col. 6.) This data is then processed by the subtractors. This is not the same as a "second ROM R-2 for similarly storing previous pixel values, being input in parallel with first ROM R-1" as set forth in claim 23. Furthermore, Hackett does not teach the input of the current pixel value to a prescribed address in a first ROM. The registers of Hackett are not disclosed as being addressed in the functioning of the scaler. Hackett discloses that the registers are input the number of needed pixels. Alternatively, the claimed invention sets forth that the "current pixel value is input to a prescribed address in said first ROM." It is clear that the pixel data forms part of the address for addressing the new pixel data which is already stored in the ROM. The ROMs set forth in the claims do not receive data values and store them as Hackett discloses. This is significant since the ROM is **Read Only Memory**. The ROMs store the pixel data and are addressed using the current pixel values. Moreover the subtractors disclosed by Hackett do not perform the addition mapping as recited in the language of the claim.

We find that the Examiner has not met the burden of setting forth a ***prima facie*** case of obviousness in rejecting claim 23. Each of the independent claims contains similar limitations as discussed above with respect to claim 23. In regard to the 35 U.S.C. § 103 rejection, the Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). Each of claims 23-26, contain the same basic limitation concerning the two ROMs, the adder and the latch. Accordingly, we will not sustain the Examiner's rejection of claims 23-26 under 35 U.S.C. § 103.

Since all the limitations of independent claims 23-26 are not suggested by the applied prior art, we cannot sustain the Examiner's rejection of appealed claims 2, 7-10, 14, 15, 17, and 27-29 which depend therefrom, under 35 U.S.C. § 103.

CONCLUSION

To summarize, the decision of the Examiner rejecting claims 7-10 under 35 U.S.C. § 112, first paragraph is reversed. The decision of the Examiner rejecting claims 2, 7-10, 14, 15 and 17 under 35 U.S.C. § 112, second paragraph is reversed. The decision of the Examiner rejecting claims 2, 7-10, 14, 15, 17, and 23-29 under 35 U.S.C.

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§ 103 is reversed. The decision of the Examiner is reversed.

REVERSED

JERRY SMITH)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
LEE E. BARRETT)	APPEALS AND
Administrative Patent Judge)	INTERFERENCES
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JOSEPH L. DIXON)	
Administrative Patent Judge)	

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Unisys Corporation, Law Dept.
2049 Century Park East
Suite 310
Los Angeles, CA 90067