

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 28

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DALE C. MORRIS, BARRY J. FLAHIVE, MICHAEL G.
ZIEGLER, JEROME C. HUCK, STEPHEN G. BURGER,
RUBY B. LEE, BERNARD L. STUMPF and JEFF KURTZEL

Appeal No. 1998-1113
Application 08/533,878

ON BRIEF

Before HAIRSTON, FLEMING, and GROSS, **Administrative Patent Judges**.

FLEMING, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-2, 4-5, and 7-8. Claims 3 and 6 were objected to as being dependent on a rejected base claim.

The invention relates to a way of protecting store operations without affecting load operations and to protection of load operations without affecting store operations. The functions are performed without requiring additional CPU time. This goal is accomplished by providing an ordered store instruction which prevents the CPU from performing its ordered store operation until preceding store operations are completed. In addition, an ordered load instruction prevents the CPU from performing subsequent load operations until its ordered load operation is completed.¹

Independent claims 1, 4 and 7 are as follows:

1. A method of ordering load operations performed by a CPU executing a stream of instructions, wherein the stream of instructions are in a program order and include load instructions and store instructions, and the load instructions each perform a load operation, the method comprising:

detecting an ordered load instruction in the stream of instructions;

preventing the CPU from executing a load instruction subsequent in the program order to the ordered load instruction prior to the load operation requested by the ordered load instruction being completed by the CPU; and

allowing the CPU to not execute a load instruction preceding in the program order the ordered load instruction

¹ See pages 4-5 and 11-12 of the specification.

prior to the load operation requested by the ordered load instruction being completed by the CPU.

4. A method of ordering store operations performed by a CPU executing a stream instruction, wherein the stream of instructions are in a program order and include load instructions and store instructions, and the store instructions each perform a store operation, the method comprising:

detecting an ordered store instruction in the stream of instructions;

preventing the CPU from executing the ordered store instruction before the store operations requested by all store instructions preceding in the program order the ordered store operation are completed by the CPU and;

allowing the CPU to execute a store instruction subsequent in the program order to the ordered store instruction prior to the store operation requested by the ordered store instruction being completed by the CPU.

7. A digital computer having an instruction execution means for executing instructions from a stream of instructions, including load and store instructions, wherein the stream of instructions are in a program order, the digital computer comprising:

detection means for detecting an ordered store or an ordered load instruction in the stream of instructions; and

control means, connected with the detection means, to control the instruction execution means as follows:

if an ordered load instruction is detected, the control means controls the instruction execution means such that a load instruction subsequent in the program order to the ordered load instruction is not executed prior

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to the ordered load instruction load being
completed by the instruction execution means,
while execution of load instructions preceding
in the program order the ordered store
instruction need not occur before execution of
the ordered load instruction is completed; or

if an ordered store instruction is detected, the
control means controls the instruction execution
means such that the ordered store instruction is not
executed prior to a store instruction preceding in
the program order the ordered store operation being
completed, while execution of store instructions
subsequent in the program order is allowed.

The Examiner relies on the following reference:

Frailong et al. (Frailong) 5,265,233 Nov. 23, 1993

Claims 1-2, 4-5, and 7-8 are rejected under 35 U.S.C. §
103 as being unpatentable over Frailong. Appellants have
indicated that claims currently under appeal fall into three
groups: Group 1, claims 1-2; Group 2, claims 4-5; and Group 3,
claims 7-8. Rather than reiterate all arguments of
Appellants and Examiner, reference is made to the briefs and
answer for the respective details thereof.²

² See the briefs filed August 29, 1997 and October 31, 1997 and answer mailed September 30, 1997. An office communication was mailed November 13, 1997 stating that the brief filed October 31, 1997 had been entered.

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OPINION

We will not sustain the rejection of claims 1-2, 4-5, and 7-8 under 35 U.S.C. § 103.

As pointed out by our reviewing court, we must first determine the scope of the claim. "[T]he name of the game is the claim." *In re Hiniker Co.*, 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998). Moreover, when interpreting a claim, words of the claim are generally given their ordinary and accustomed meaning unless it appears from the specification or the file history that they were used differently by the inventor. *Carroll Touch, Inc. V. Electro Mechanical Sys., Inc.*, 15 F.3d 1573, 1577, 27 USPQ2d 1836, 1840. Although an inventor is indeed free to define the specific terms used to describe his or her invention, this must be done with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1479, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994).

Claim 1 is directed to a method of ordering load operations. The method includes steps of detecting an ordered

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load instruction and preventing the CPU from executing later load instructions until execution of the ordered load instruction is completed. All earlier load instructions need not be executed before the execution of the ordered load instruction is complete. Claim 4 is directed to a method of ordering store operations. The method includes steps of detecting an ordered store instruction and preventing the CPU from executing the ordered store instruction until all earlier store instructions have been completely executed. A later store instruction can be executed before execution of the ordered store instruction is completed. Earlier or later store instructions are relative to the ordered store instruction. Finally, claim 7 makes use of an ordered store instruction or an ordered load instruction for executing instructions from a stream of instructions.

The Examiner has failed to set forth a *prima facie* case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or

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suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordance Mfg. V. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***cert. denied***, 117 S. Ct. 80 (1996) ***citing W. L. Gore & Assocs., Inc. V. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984).

Frailong discusses the STBAR operations in col. 11, line 55, to col. 12, line 5. In this passage, Frailong discloses that "processor 104 waits until all Store operations that were issued to the External Cache of that processor prior to the STBAR operations have completed execution before allowing subsequent Store operations to appear on the processor bus . . . all Store instructions issued before a STBAR instruction must complete execution before any of the Store instructions that were issued after a STBAR instruction." The reference clearly discusses the relationship between the order in which instructions before the STBAR instruction and those appearing

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after the instruction are executed. It does not, however, disclose any relationship between the order in which an instruction appearing before or after the STBAR instruction and the STBAR instruction itself is executed.

Claims 1, 4, and 7 clearly recite limitations on the order of execution of the ordered store/load instruction and store/load instructions appearing before or after the ordered instruction.³

As the examiner has failed to recognize and account for the differences as printed out above, the rejection of claims 1, 4, 7, and any claims depending therefrom cannot be sustained.

For these reasons, the rejection of claims 1-2, 4-5, and 7-8 under 35 U.S.C. § 103 is reversed.

REVERSED

³ See lines 10-12 of claim 1; lines 10-12 of claim 4; and lines 9-20 of claim 7.

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