

The opinion in support of the decision being entered today was not written for publication in a law journal and is not binding precedent of the Board.

Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte FERAYDOON S. JAMZADEH

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Appeal No. 1998-0940  
Application No. 08/085,605

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ON BRIEF

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Before HAIRSTON, KRASS and JERRY SMITH, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 3, 4, 7, 12 and 14-16. The rejection of claims 5 and 6 is not appealed.

The invention is directed to a raster image processor. In particular, an interpolator is used to increase the speed of operation and to reduce memory requirements for electronic printing. More specifically, coded instructions in a page

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description file (PDL) are decoded at a first resolution to generate a first bit-mapped field of image data and the bit-mapped field is stored in a frame-store. The bit-mapped field of image data is fed to an interpolator which operates in real time to interpolate the bit-mapped field to a second resolution, higher than the first resolution. The higher resolution interpolated data is used to expose a first image frame on a recording member and, while data for one image frame is being output from the frame-store's memory and being interpolated and being printed, data for a second image frame is being input into the same frame-store that is currently outputting data of the prior image frame. It is said that the invention reduces bandwidth requirements for transferring data between the raster image processor (RIP) and the frame-store and reduces the processing time of the RIP since data is processed by the RIP at the lower resolution.

Representative independent claim 4 is reproduced as follows:

4. A document generation method for providing an output image having full printing resolution said method comprising the steps of:

(a) receiving a set of image data having coded instructions in a page description language;

(b) decoding said coded instructions in said image data at a first resolution;

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(c) generating a first bit-mapped field of image data according to the coded instructions of the page description language for recording on a first image frame;

(d) storing the bit-mapped field in a frame-store;

(e) outputting the bit-mapped field of image data from the frame-store to an interpolator;

(f) interpolating the bit-mapped field of image data in real time to a second resolution higher than the first resolution;

(g) exposing a first image frame of an image sensitive media with the interpolated bit-mapped field of image data;

(h) repeating steps (a) and (b) for a different set of image data to generate a second bit-mapped field of image data according to the coded instructions of the page description language for recording on a second image frame; and

(i) inputting the second bit-mapped field of image data in said frame-store while performing steps (e), (f) and (g) on said first bit-mapped field of image data.

The examiner relies on the following references:

Suzuki	4,722,064	Jan. 26, 1988
Reisch et al. (Reisch)	5,168,375	Dec. 01, 1992
Shimura et al. (Shimura)	5,206,741	Apr. 27, 1993
Kadowaki et al. (Kadowaki)	5,351,074	Sep. 27, 1994

(filed Oct. 13, 1992)

Claims 3, 4, 7, 12 and 14 stand rejected under 35 U.S.C.

103. As evidence of obviousness, the examiner employs four different combinations of Kadowaki, Suzuki and Shimura. Claims 15 and 16 also stand rejected under 35 U.S.C. 103, with Reisch being added to the combination of Kadowaki, Suzuki and Shimura as evidence thereof.

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Reference is made to the briefs and answers for the respective positions of appellant and the examiner.

OPINION

In a new ground of rejection, entered in the principal answer (paper No. 13), the examiner first states that Kadowaki discloses the invention as substantially claimed except that Kadowaki only teaches enlarging resolution to a second higher resolution in some unspecified manner rather than generating a second higher resolution by "interpolating," as claimed. The examiner relies on Shimura for generating a second higher resolution by such "interpolating" and holds that it would have been obvious to choose interpolating for the unspecified type of enlarging in the system of Kadowaki "for the advantages associated with interpolation such as maintaining or increasing image quality with minimal processing overhead" (principal answer, page 5).

Alternatively, the examiner finds that Suzuki discloses the invention as substantially claimed but for the generation of a second higher resolution by interpolating. Again, the examiner relies on Shimura to provide such a teaching and holds that it would have been obvious to combine Suzuki and Shimura "for the

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advantage of enlarging printing resolution with out [sic, without] increasing memory size" (principal answer, page 5).

The examiner employs a third combination of all three of these references in rejecting claims 3, 4, 7, 12 and 14 under 35 U.S.C. § 103, finding now that Shimura discloses the invention but for the "while" limitation, i.e., that the step of inputting the second bit-mapped field of image data in the frame-store is performed "while" performing steps (e), (f) and (g) on the first bit-mapped field of image data. The examiner then relies on Kadowaki and Suzuki for teaching the performance of writing/ inputting associated functions for a second image while performing reading/outputting associated functions for a first image of a bit-mapped memory, as claimed. In the examiner's view, it would have been obvious to adapt the system of Shimura to perform reading/outputting associated functions while performing writing/inputting functions "in order to obtain the advantage higher operating speeds that would result" [sic] (principal answer, page 6).

The examiner produces a table, at pages 7-12 of the principal answer, purporting to show the correspondence between the claimed elements and the elements disclosed by the references.

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Appellant points out, in the reply brief, very specific claimed elements which are not taught or suggested by the references. With regard to claim 4, it is required that the bit-mapped field is interpolated, in real time, to a "second" resolution higher than a first resolution and that some of the claimed steps are repeated for a different set of image data to generate a second bit-mapped field of image data for recording on a second image frame and inputting the second bit-mapped field into the same frame-store used for storing the first bit-mapped field "while" performing the steps of outputting the bit-mapped field from the frame-store to an interpolator, interpolating the bit-mapped field in real time to a second resolution higher than the first resolution and exposing the first image of an image sensitive media with the interpolated bit-mapped field.

While Shimura teaches different resolutions based on memory space, it does not disclose the simultaneous writing to a single frame-store memory of one image frame of data "while" reading a prior image frame's data out of that same memory, and then interpolating the data and printing. With regard to Kadowaki, appellant points out that this reference discloses the storing of color separation data by first clearing a full page image memory and that color separation data for one page is input into one of

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the page memories while printing of image data is output from another of the page memories. Note the two full page memories 104-1 and 104-2. Appellant concludes that Kadowaki "teaches away" from the claimed subject matter by clearing a bit-map memory before sending data to that memory. Appellant notes that Suzuki is similar to Kadowaki.

We have reviewed the evidence and we conclude that appellant is correct in that Kadowaki, Shimura and Suzuki appear to be all deficient in failing to disclose or suggest the *simultaneous* reading and writing of different frames of bit-mapped image data from the *same* frame-store as specifically set forth in each of the instant claims on appeal. We note that in response to these arguments by appellant, the examiner, in a supplemental answer (Paper No. 13), merely refers back to pages 5, 6, 8, 9 and 10-12 of the principal answer, addressing the "while" limitation. We do not find the examiner's arguments convincing in light of the deficiencies of the references as indicated by appellant. The examiner alleges that both Suzuki and Kadowaki teach the performance of writing/inputting associated functions for a second image while performing reading/outputting associated functions for a first image of a bit-mapped memory but fails to point to any specific portions of these references where the

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alleged feature is taught. Further, the examiner has not convincingly pointed to anything in the applied references regarding storing the bit-mapped field in "a" frame-store and subsequently inputting second bit-mapped field of image data in that "same" frame-store.

Thus, we will not sustain the rejection of claims 3, 4, 7, 12 and 14 under 35 U.S.C. § 103.

Since the reference to Reisch does not remedy the deficiencies of the other applied references, we also will not sustain the rejection of claims 15 and 16 under 35 U.S.C. § 103.

Accordingly, the examiner's decision is reversed.

REVERSED

KENNETH W. HAIRSTON	)	
Administrative Patent Judge	)	
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ERROL A. KRASS	)	BOARD OF PATENT
Administrative Patent Judge	)	APPEALS AND
	)	INTERFERENCES
	)	
	)	
JERRY SMITH	)	
Administrative Patent Judge	)	

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