

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte FREDERIC BOUTARD
and PETER N. EHLIG

Appeal No. 1998-0049
Application 08/289,028¹

ON BRIEF

Before MARTIN, BARRETT, and GROSS, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

¹ Application for patent filed August 10, 1994, entitled "A Data Processing Device With Mask And Status Bits For Selecting A Set Of Status Conditions," which is a division of Application 07/967,942, filed October 28, 1992, now abandoned.

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This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 61-63, 65-70, 72, 74-76, 81, and 88-93.

We affirm-in-part.

BACKGROUND

The disclosed invention relates to an instruction format for a data processing device, as described in the specification at page 103, line 26 to page 109, line 18. The instruction is provided with a field for mask bits for specifying a particular set of status conditions which are to be used for a conditional test; the function performed by the instruction is then determined by the result of the conditional test. The instruction may have status bits that, taken together with the mask bits, determine a conjunction of conditions; see figure 32 and the accompanying discussion.

Claim 61 is reproduced below.

61. A data processing device comprising:

a circuit having status conditions wherein a particular set of the status conditions can occur in operation of the circuit;

an instruction register operative to hold a predetermined instruction conditional on a particular

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set of the status conditions and includes locations for mask bits to select any one or more of the conditions to form said particular set of status conditions;

a decoder connected to said instruction register and said circuit; and

circuitry to perform a predetermined function in response to the predetermined instruction when said particular set of the status conditions of said circuit are present.

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The Examiner relies on the following prior art:

| | | |
|------------------------------------|-----------|---|
| Vandierendonck et al. 1976 | 3,987,416 | October 19, |
| (Vandierendonck) | | |
| Itomitsu et al. (Itomitsu) 1995 | 5,440,704 | August 8, |
| | | (effective filing date July 9, 1990) |

Claims 61-63, 65-70, 72, 74-76, 81, and 88-93 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Itomitsu and Vandierendonck.

We refer to the Final Rejection (Paper No. 7) (pages referred to as "FR__") and the Examiner's Answer (Paper No. 13) (pages referred to as "EA__") for a statement of the Examiner's position, and to the Brief (Paper No. 12) (pages referred to as "Br__") and the Reply Brief (Paper No. 14) (pages referred to as "RBr__") for a statement of Appellants' arguments thereagainst.

OPINION

Grouping of claims

Appellants state that the claims may be considered as one group, i.e., as standing or falling together, but that claims 63 and 88 are separately patentable (Br4). Appellants separately argue claims 63 and 88 (Br6).

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Therefore, we agree with Appellants' argument (RBr2) that the Examiner erred in stating that claims 63 and 88 are not argued as separately patentable (EA3). However, we note that the Examiner's Answer does mention claims 63 and 88 (at EA9).

For claims that are grouped as standing or falling together, the normal procedure is to select a single claim from the group and to decide the appeal as to the ground of rejection on the basis of that claim alone. See 37 CFR § 1.192(c)(7) (1999). Claim 61 is the broadest of the independent claims and is analyzed as the representative claim. Claim 61 only requires the predetermined instruction to include locations for mask bits, as compared to claims 74 and 81 in which the instruction includes both mask bits and status bits. Normally, we do not question an applicant's grouping of claims. Thus, we ordinarily would not consider claims 74 and 81 separately or regroup them even though they appear closer to the scope of dependent claim 63, which is argued separately, than to independent claim 61. In this case, however, because we apply different reasoning on the same references, as discussed infra, to be fair, we will not

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treat claims 74 and 81 as standing or falling together with claim 61.

Obviousness

Claims 61, 62, 65-70, and 89

The Examiner finds that Itomitsu generally teaches the limitations of the claims, except "Itomitsu did not teach instruction register including mask bits but Vandierendonck et al (3,987,416) taught instruction register including mask bits (figure 5)" (FR3-4; EA6). The Examiner concludes that it would have been obvious to combine the teachings of Itomitsu and Vandierendonck "because they were both directed toward providing circuits for executing conditional instructions and mask fields of Vandierendonck et al would improve execution and computation speed of Itomitsu et al" (FR4; EA6).

The issue is whether Vandierendonck discloses or suggests the limitations of "mask bits to select any one or more of the conditions to form said particular set of status conditions" and "circuitry to perform a predetermined function in response to the predetermined instruction when said particular set of the status conditions of said circuit

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are present," which require conditional execution of an instruction depending on the set of status conditions selected by the mask bits.

Appellants generally agree with the Examiner's characterization of the teachings of Itomitsu (Br4) and, hence, we will not further discuss the reference.

Appellants argue that the four bit "mask" field in Vandierendonck selects one of 16 digit masks in the encoder and decoder arrays of digit mask logic 35, as described at col. 13, line 12 to col. 14, line 9, and thus "Vandierendonck's 'mask' is actually in the encoder and decoder arrays, and not in the instruction, as claimed by Appellants" (Br5).

We do not find where the Examiner clearly answers this argument. Nevertheless, claim 61 does not expressly require a one-to-one correspondence between mask bits and status conditions and, therefore, claim 61 does not preclude the mask bits from being encoded mask bits that are decoded to produce the actual mask bits to be used to select status conditions.

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Appellants further argue (Br5) that they find no teaching in Vandierendonck of utilizing the mask bits "to select any one or more of the conditions to form said particular set of status conditions," as claimed. It is argued that Vandierendonck's "mask" is used only in register and flag instructions for encoding and decoding digits for ALU manipulation and display, not for conditional branch instructions (Br5).

The Examiner responds (EA8-9):

Vandierendonck et al in columns 6-7 taught 9 bits in the instruction register are used for jump instructions, **mask logic (35) received mask bits** from the instruction register and condition logic (40) **for executing conditional branch instructions in response to various operating situations** (states or conditions e.g., see column 7 (line 1 et seq.)). Examiner cannot see any better and clearer teaching than this as far as using mask bits for branching. . . . **Vandierendonck et al** teachings with respect to using masking for conditional branch instruction is crystal clear and no one can interpret it away or argue it away. [Emphasis in original.]

Appellants respond to this new point of argument by stating that Vandierendonck does not combine masks and conditional instruction execution in any manner (RBr2). Vandierendonck's conditional jump instruction does not contain a mask field at all. It is argued that

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Vandierendonck uses a mask field for selecting display segments during a register instruction, but not for conditional execution of an instruction (RBr2).

We agree with Appellants' findings regarding the teachings of Vandierendonck as applied by the Examiner. While figure 5 of Vandierendonck discloses mask bits, these mask bits are only used for the flag and register instructions, not the jump instructions. The mask bits in the flag and register instructions are not used to select any of the conditions in the condition logic 40, but are used to produce constants in the digit mask logic 35 for use in connection with the sequentially addressed memory (SAM) 20 (col. 13, line 12 to col. 14, line 9). The Examiner's response, quoted supra, fails to distinguish between the conditional branch instructions, which do not have mask bits but are responsive to status conditions, and the flag/register instructions, which do have mask bits but are not responsive to status conditions. Accordingly, the Examiner's rationale is erroneous.

However, it appears that claim 61 is anticipated by Vandierendonck when the bits of the "class field," I9 and

I10, are considered to be the "mask bits" of claim 61. The label attached to the bits is not of patentable significance. The circuit of Vandierendonck has a set of status conditions that can occur in operation, e.g., a flag condition or a keyboard input can set or reset a condition latch 47 in input and condition logic 40 (col. 6, line 67 to col. 7, line 4). Vandierendonck has an instruction register 31 (figure 2) which can hold four jump instructions (figure 5) conditional on a particular set of status conditions selected by the "class field" bits. For example, if the "condition" is whether the condition latch is "set" or "reset," the class field 00 causes a jump if the condition latch is reset and the class field 01 causes a jump if the condition latch is set. Thus, the "class field" bits perform the same function as Appellants' "mask bits." The instruction register 31 is connected to the input and condition logic circuit 40. Circuitry causes the address of the next instruction at bits I0 to I8 to be loaded from the instruction register 31 to the address registers 36, 37 if the condition specified by the "class field" bits is satisfied (col. 7, lines 4-11). Therefore, we sustain the

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rejection of claims 61, 62, 65-70, and 89, albeit on different reasoning.

Claims 63, 72, 74-76, 81, and 90-93

Dependent claim 63 additionally recites "status bits corresponding to said mask bits to determine the way in which a status condition selected by each of said mask bits is interpreted." Independent claims 74 and 81 contain similar limitations. The Examiner's rejection does not address these limitations. Vandierendonck does not disclose or suggest status bits which are used in conjunction with the mask bits. The Examiner has failed to establish a prima facie case of obviousness. Therefore, the rejection of claims 63, 72, 74-76, 81, and 90-93 is reversed.

Claim 88

Claim 88 recites a program counter and entering a branch address into the program counter in response to the branch instruction when the particular set of status conditions selected by the mask bits are present. Appellants argue that Vandierendonck's "mask" field has nothing to do with selecting a set of status conditions to

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be used to condition a branch instruction (Br6). This is true. However, under our interpretation of the "class bits" as the "mask bits," the "class bits" do select a status condition to condition a branch instruction. Circuitry causes the address of the next instruction to be loaded from the instruction register 31 to the address registers 36, 37 if the condition specified by the "class bits" is satisfied (col. 7, lines 4-11), where the address registers are considered the program counter. Therefore, we sustain the rejection of claim 88.

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CONCLUSION

The rejection of claims 61, 62, 65-70, 88, and 89 is sustained.

The rejection of claims 63, 72, 74-76, 81, and 90-93 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

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| | JOHN C. MARTIN |) | |
| | Administrative | Patent Judge |) |
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| | LEE E. BARRETT |) | APPEALS |
| | Administrative | Patent Judge |) |
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