

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 26

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DANIEL F. CASPER,
JAMES T. BRADY,
ROBERT S. CAPOWSKI,
FREDERICK J. COX,
FRANK D. FERRAIOLO,
MARTEN JAN HALMA,
and BENJAMIN H. WU

Appeal No. 1997-4125
Application No. 08/261,523

ON BRIEF

Before URYNOWICZ, FLEMING, and BARRY, Administrative Patent Judges.

BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the final rejection of claims 1-3. The appellants filed a first amendment after final rejection on December 17, 1996,

and second amendment after final rejection on May 4, 1997.
Both were entered. We reverse.

BACKGROUND

Manufacturing tolerances, temperature changes, and power variations have limited the useful length of a parallel computer bus operating at high data rates. In a computer that transfers data synchronously with respect to a system clock, moreover, changing the rate of the clock has required redesigning the bus.

The invention at issue in this appeal is a self-timed interface (STI) that transfers data between a host processor and a peripheral controller. More specifically, the STI clocks data onto lines of a parallel computer bus while transmitting the clock signal on another line of the bus. Upon receipt, the data on each line are individually phase-aligned with the clock signal, thereby compensating for manufacturing tolerances, temperature changes, and power variations. Consequently, the maximum length of the bus is limited only by its attenuation loss. The bus can operate at

high data rates, moreover, without tight control of its length
and without clock constraints.

Claim 1, which is representative for our purposes,
follows:

1. A data processing system comprising in combination:
 - a host processor;
 - a peripheral controller;
 - an input-output sub-element physically located remotely from said host processor;
 - a self-timed interface link coupling host commands and data directly between said host processor to said input-output sub-element and said peripheral controller;
 - said self-timed interface link including a transmitting node for transmitting a digital data and a clock signal and a receiving node for receiving said digital data and said clock signal, said transmitting node connected to said receiving node by a parallel data bus to individual lines of which respective bits of digital data streams are coupled in parallel by said clock signal at said transmitting node; and
 - said bus including a separate line for transmitting said clock signal to said receiving node, and said receiving node including means to phase align said respective bits on each of said lines separately with respect to said clock signal transmitted to said receiving node.

The references relied on in rejecting the claims follow:

Read et al. (Read)	4,885,739	Dec. 5, 1989
Murakami et al. (Murakami)	5,113,395	May 12, 1992
Cisneros et al. (Cisneros)	5,166,926	Nov. 24, 1992

Claims 1-3 stand rejected under 35 U.S.C. § 103(a) as obvious over Read in view of Cisneros further in view of Murakami. Rather than repeat the arguments of the appellants or examiner in toto, we refer the reader to the briefs and answers for the respective details thereof.

OPINION

In reaching our decision in this appeal, we considered the subject matter on appeal and the rejections advanced by the examiner. Furthermore, we duly considered the arguments and evidence of the appellants and examiner. After considering the totality of the record, we are persuaded that the examiner erred in rejecting claims 1-3. Accordingly, we reverse.

At the outset we note that the examiner once rejected claims 1-3 under 35 U.S.C. § 112, ¶ 1. He observed, "The feature 'simultaneously' claim 1, line 15, claims 2, line 24 and claim 3, line 25 [sic] was not disclosed in the originally filed specification" (First Supplemental Examiner's Answer at 3.)

A rejection not referred to in an examiner's answer is assumed to have been withdrawn. Ex parte Emm, 118 USPQ 180, 181 (Bd. Pat. App. & Int. 1958) (citing Ex parte Charch, 102 USPQ 363, 364 (Bd. Pat. App. & Int. 1954) and Ex parte Hill, 93 USPQ 45, 46 (Bd. Pat. App. & Int. 1952)). In the subsequent and final examiner's answer, viz., the Second Supplemental Examiner's Answer (Paper No. 19), the examiner neither repeats nor references the rejection under 35 U.S.C. § 112, ¶ 1. He only discusses the obviousness rejection therein. Therefore, we conclude that the rejection under 35 U.S.C. § 112, ¶ 1 has been withdrawn.

Considering the rejection on its merits arguendo, however, we note that the term "simultaneously" has been deleted from the claims. (Paper No. 18 at 2-4.) Because the rejection was based on the addition of the term to the claims, its deletion renders the rejection moot. Next, we address the obviousness of the claims.

We begin by noting the following principles from In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993).

In rejecting claims under 35 U.S.C. § 103, the examiner bears the initial burden of presenting a prima facie case of obviousness. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). Only if that burden is met, does the burden of coming forward with evidence or argument shift to the applicant. Id. "A prima facie case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." In re Bell, 991 F.2d 781, 782, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting In re Rinehart, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)). If the examiner fails to establish a prima facie case, the rejection is improper and will be overturned. In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

With these in mind, we address the appellants' argument.

The appellants make the following argument.

There is no teaching or suggestion within these references that would lead one of ordinary skill in the art to combine them in the manner proposed by the Examiner. Moreover, even if they were so combined, the resultant combination would still lack the claimed structure wherein the receiving node includes means to phase align the digital data stream on each of the parallel bus lines separately with respect to the separately transmitted clock

signal which was used to clock the data onto the individual lines of the bus at the transmitting node. (First Reply Br. at 8.)

The examiner replies, "it would have been obvious ... to provide for a clock signal with the means to phase align input data to allow the use of clock signals with different rates and to reduce framing errors." (Examiner's Answer to Reply Brief at 6.)

"[T]he main purpose of the examination, to which every application is subjected, is to try to make sure that what each claim defines is patentable. [T]he name of the game is the claim'" In re Hiniker Co., 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998) (quoting Giles S. Rich, The Extent of the Protection and Interpretation of Claims --American Perspectives, 21 Int'l Rev. Indus. Prop. & Copyright L. 497, 499, 501 (1990)). Here, claims 1-3 each specify in pertinent part the following limitations:

said self-timed interface link including a transmitting node for transmitting a digital data and a clock signal and a receiving node for receiving said digital data and said clock signal, said transmitting node connected to said receiving node by a parallel data bus to individual lines of which respective bits of digital data streams are

coupled in parallel by said clock signal at said transmitting node; and

said bus including a separate line for transmitting said clock signal to said receiving node, and said receiving node including means to phase align said respective bits on each of said lines separately with respect to said clock signal transmitted to said receiving node.

In short, the claims each recite individually phase-aligning data bits transmitted on lines of a bus with respect to a clock signal transmitted along with the data on another line of the bus.

The examiner fails to show a teaching or suggestion of the claimed limitation. "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." Para-Ordnance Mfg. v. SGS Importers Int'l, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), cert. denied, 519 U.S. 822 (1996) (citing W.L. Gore & Assocs., Inc. v. Garlock, Inc., 721 F.2d 1540, 1551, 1553, 220 USPQ 303, 311, 312-13 (Fed. Cir. 1983)). "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art

suggested the desirability of the modification." In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992) (citing In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)). "It is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior

art so that the claimed invention is rendered obvious." Id.
at 1266, 23 USPQ2d at 1784, (citing In re Gorman, 933 F.2d
982, 987, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991)).

Here, the examiner admits, "Read does not explicitly
disclose ... that the clock signal with the means to align is
phase aligned." (Second Supplemental Examiner's Answer at 3.)
This is an understatement. The reference merely teaches
synchronizing clocks with data. Specifically, "timing islands
provide levels at which the clocks are synchronized with the
data, in order to prevent skewing between the timing used
by various subsystems." Col. 2, ll. 8-11.

The examiner fails to allege, let alone show, that
Cisneros remedies the defects of Read. He instead relies on
Murakami to "disclose that the clock signal with the means to
align is phase aligned" (Second Supplemental Examiner's
Answer at 3.) Although the latter reference teaches phase-
aligning, it does not teach individually phase-aligning data
bits transmitted on lines of a bus with respect to a clock
signal transmitted along with the data on another line of the

bus. Rather than phase-aligning data bits to a clock signal, Murakami's device phase-aligns a frame signal to a frame synchronous signal. Specifically, the "invention provides a device for phase-aligning an input time-division multiplexed signal having an input clock signal to an output frame synchronous signal synchronized with an output clock signal different from the input clock signal to produce an output frame signal" Col. 2, ll. 63-68.

Because the references do not teach phase-aligning data bits to a clock signal, we are not persuaded that teachings from the prior art would appear to have suggested the claimed limitation of phase-aligning data bits transmitted on lines of a bus with respect to a clock signal transmitted along with the data on another line of the bus. The examiner has impermissibly relied on the appellants' teachings or suggestions; he has not established a prima facie case of obviousness. Therefore, we reverse the rejections of claims 1-3 under 35 U.S.C. § 103(a).

CONCLUSION

To summarize, the rejection of claims 1-3 under 35 U.S.C.
§ 103(a) is reversed.

REVERSED

STANLEY M. URYNOWICZ, JR.)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
MICHAEL R. FLEMING)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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LANCE LEONARD BARRY)	
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Page 14

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