

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte FUMIHIRO NAGASAWA

Appeal No. 1997-4034
Application No. 08/260,269

ON BRIEF¹

Before KRASS, LALL, and GROSS, Administrative Patent Judges.
GROSS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1 through 12, which are all of the claims pending in this application.

Appellant's invention relates to a video signal recording apparatus in which the read control signal for reading the video signal stored in memory is synchronized with a timing

¹ We observe that on September 29, 2000 (paper no. 23), appellant filed a waiver of the oral hearing set for November 15, 2000.

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signal relating to the driving state of the recording means.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A video signal recording apparatus for recording a video signal on a recording medium, comprising:

memory means for storing said video signal at a time in accordance with a write control signal;

synchronizing separating means for separating a synchronizing signal from said video signal;

write control signal generating means for generating said write control signal in response to said synchronizing signal;

recording means for recording said video signal read out from said memory means on said recording medium;

timing signal generating means for generating a timing signal relating to a driving state of said recording means; and

read control signal generating means for generating a read control signal used to read said video signal stored in said memory means at a time synchronized with said timing signal.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Shimizu et al. (Shimizu) 10, 1987	4,649,438	Mar.
Yoshioka et al. (Yoshioka) 1990	4,916,553	Apr. 10,
Kanota 1993	5,212,600	May 18,

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Yamada
1994

5,293,274

Mar. 08,

Claims 1, 2, and 11 are rejected under 35 U.S.C. § 102(b) as being anticipated by Yoshioka.

Claims 3 through 9 stand rejected under 35 U.S.C. § 103 as being unpatentable. As evidence of obviousness the examiner offers Yoshioka in view of Yamada, with the addition of Shimizu for claim 7 and the addition of Shimizu considered with "official notice" for claims 8 and 9.

Claims 10 and 12 stand rejected under 35 U.S.C. § 103 as being unpatentable over Yoshioka in view of Kanota.

Reference is made to the Examiner's Answer (Paper No. 11, mailed April 15, 1996) for the examiner's complete reasoning in support of the rejections, and to appellant's Brief (Paper No. 10, filed February 21, 1996) and Reply Brief (Paper No. 12, filed June 13, 1996) for appellant's arguments thereagainst.

OPINION

We have carefully considered the claims, the applied prior art references, and the respective positions articulated by appellant and the examiner. As a consequence of our

review, we will affirm the anticipation rejection of claims 1, 2, and 11 and the obviousness rejections of claims 3 through 9, but reverse the obviousness rejection of claims 10 and 12.

The only limitation argued by appellant for claim 1 is "read control signal generating means for generating a read control signal used to read said video signal stored in said memory means at a time synchronized with said timing signal." All agree that Yoshioka discloses a timing signal relating to a driving state of the recording means and a read start signal synchronized with the timing signal. However, appellant explains (Brief, page 8) that in Yoshioka's device "the pulse value of read start pulses RS ... is latched at each pulse occurrence of read clock pulses CP_2 and the latched value, if a pulse is latched, operates to reset the address in counter 404." Appellant then concludes that "the read address signal (i.e., the output of counter 404) is synchronized with read clock pulses CP_2 , and **not** with read start pulses RS." We disagree.

In Figure 7, Yoshioka shows read start pulses (Fig. 7f) synchronized with the read address controller output (Fig. 7i) and also with the tach pulses, or the timing signal relating

to the driving state of the recording means. Thus, in our view, Figure 7 indicates that the read address signal is synchronized with the timing signal.

The examiner states (Answer, page 4) that since Yoshioka discloses that the read start pulses are synchronized with both the tach pulses and the read clock pulses CP_2 , and the read control signal is synchronized with the read clock pulses CP_2 , the read control signal is also synchronized with the tach pulses. Appellant, on the other hand, argues (Reply Brief, page 3) that although the read start pulses are initially synchronized with the rotary heads, when they become synchronized with the read clock pulses CP_2 by the latch circuit, the output of the latch circuit (i.e. the read control signal) is only synchronized with read clock pulses CP_2 . However, as explained above, Figure 7 of Yoshioka evidences that the read control signal is synchronized with both the read start and the tach pulses. Accordingly, we will affirm the anticipation rejection of claims 1 and 2.

Claim 11 recites a step of generating a read control signal in accordance with the timing signal. Thus, the method step of claim 11 parallels the device limitation discussed

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above for claim 1. Accordingly, we will affirm the anticipation rejection of claim 11 for substantially the same reasons set forth above regarding the rejection of claim 1.

As to claims 3 through 9, although the examiner added Yamada (for rejecting claims 3 through 6) and further added Shimizu (for rejecting claims 7 through 9), appellant (Brief, page 10) rests all arguments upon the alleged deficiency of Yoshioka. Since we have found Yoshioka to contain the contested limitation, and appellant provides no arguments concerning the applicability of the additional references, we will affirm the obviousness rejections of claims 3 through 9.

On the other hand, as to claims 10 and 12, we agree with appellant (Reply Brief, page 4) that the combination of Yoshioka and Kanota would not yield a read control signal generated only from a timing signal. Yoshioka generates the read control signal from the read clock pulses and the read start signal (which is synchronized with the timing signal). Kanota generates a read control signal from a clock signal from reference oscillator 7, which is different from the claimed timing signal. Accordingly, neither reference suggests generating the read control signal from only the

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recited timing signal. Therefore, we will not sustain the obviousness rejection of claims 10 and 12.

CONCLUSION

The decision of the examiner rejecting claims 1, 2, and 11 under 35 U.S.C. § 102(b) is affirmed. The decision of the examiner rejecting claims 3 through 9 under 35 U.S.C. § 103 is affirmed. The decision of the examiner rejecting claims 10 and 12 under 35 U.S.C. § 103 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

ERROL A. KRASS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
PARSHOTAM S. LALL)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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