THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

_____

Ex parte RICHARD SIMPSON,
KEITH BALMER,
and
IAIN ROBERTSON

_____

Appeal No. 1997-3818
Application 08/208,517[1]

_____

ON BRIEF

_____

[1] Application for patent filed March 8, 1994.

Before MARTIN, FLEMING and BARRY, ***Administrative Patent Judges***.

MARTIN, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1-4, 11, and 12 under 35 U.S.C. § 103.[2] Claims 19-36, the only other pending claims, stand allowed. We affirm-in-part.

A. The invention

Appellants' summary of the invention, which the examiner indicates (Answer at 2) is correct, reads in pertinent part as follows:

> This invention is a data processing apparatus (100) which may interface with plural types of memories. A static decoder coupled to an external port (302) decodes signals (address shift selection AS[2:0], bus size selection BS[1:0], column timing selection CT[1:0], page size selection PS[2:0], and **&&&&&** inputs) which from [sic] an external source that indicate the

[2] The other grounds of rejection stated in the final rejection and the Answer were withdrawn at page 2 of the Supplemental Examiner's Answer (paper No. 18) and pages 2 and 3 of the Second Supplemental Examiner's Answer (paper No. 20).

> type of memory (page 73, lines 5 to 22). Interface circuitry (80) receives coded information from the static decoder and selects a protocol for information transfer. In the preferred embodiment, the protocol includes addressing information having multiplexed row/column addresses for accessing dynamic memories or un-multiplexed addresses for accessing static memories.
>
> . . . .
>
> The data processing apparatus (100) may also control the number of bits transferred. An external part (302) supplies a bus size signal (BS[1:0]) to a static decoder. The internal data bus is coupled to an external data bus of selectable size. The interface circuitry selects a bus size protocol based upon the received bus size signal (BS[1:0]). Thus the data processing apparatus may establish the size in bits of data transfers to accommodate the selected bus size. An endian mode memory store[s] an indication of a big endian mode or a little endian mode. The number of bits transferred is based upon the data bus size signal (BS[1:0]) but the identity of the data bus lines used is based upon the current endian mode (page 165, line 20 to page 169, line 19, Tables 24a, 24b, 25a, 25b, 26, 27, 28 and 29). [Brief at 2-3.]

B. The claims

Claims 1 and 11, the only independent claims, read as follows:

1. An image processor comprising:

a data processor having a plurality of first address lines and a plurality of first data lines, said data processor supplying an address on said plurality of first address lines and transferring data via said plurality of data lines;

an external port having a plurality of second address lines, a plurality of second data lines, a plurality of memory control output lines and a plurality of memory protocol input lines; and

a static decoder coupled to said memory protocol input lines of said external port for sampling inputs on said memory protocol input lines at a predetermined time in a memory cycle

and for decoding said sampled inputs from said memory protocol input lines of said external port into memory type signals; and

memory interface circuitry coupled to said data processor, said external port and said static decoder operative to transfer information between said data processor and said external port, said memory interface circuitry including:

an addressing means receiving a data processor address on said plurality of first address lines of said data processor and supplying said processor address to said plurality of second address lines of said external port for output;

a memory-type decoder connected to said static decoder for selecting a memory protocol for information

transfer between said data processor and said external port dependent upon said memory type signals; and

a memory controller connected to said memory type controller, said first plurality of data lines of said data processor, said second plurality of data lines and said plurality of memory control output lines of said external port for supplying memory control outputs signals to plurality of memory control output lines of said external port for control of information transfer between said data processor and said external port for a next memory cycle corresponding to said selected memory protocol.

11. A [sic] image processor comprising:

a data processor having a plurality of first address lines and a plurality of first data lines, said data processor supplying an address on said plurality of first address lines and transferring data via said plurality of data lines;

an external port having a plurality of second address lines, a plurality of second data lines, a plurality of memory control output lines and a plurality of bus size input lines; and

a data buffer connected to said first data lines of said data processor; and

memory interface circuitry coupled to said data processor, to said external port and to said data buffer operative to transfer information between said data processor and said external port, said memory interface circuitry including:

an addressing means receiving a data processor address on said plurality of first address lines of said data processor and supplying said data processor address to said

plurality of second address lines of said external port for output;

a decoding circuit connected to said bus size input lines for sampling input on said bus size input lines at a predetermined time in a memory cycle following supply of said data processor address for decoding said sampled inputs from said bus size input lines of said external port to indicate a bus size protocol for transfers of information;

a data circuit supplying data from said data buffer to a predetermined set of said second address lines of said external port corresponding to said bus size indicated by said bus size input lines in a quantity of bits corresponding to said bus size indicated by said bus size input lines and supplying no data on other of said second address lines of said external port.

We note that neither the examiner nor appellants have explained how each of the limitations of appellants' claims, including the limitations specifically argued in the brief (i.e., the "status decoder" of claim 1 and the "decoding circuit" of claim 11), read on appellants' disclosed apparatus. The only elements of claims 1 and 11 that have been read by appellants on their disclosure are the following (Brief at 2-3):

(a) the claimed "data processing apparatus" is read on data multi-processor integrated circuit 100 (Figs. 1 and 2);

(b) the claimed "external port" is read on external memory interface 302 (Fig. 8); and

(c) the claimed "interface circuitry" is read on transfer controller 80 (Figs. 2 and 8).

C. The references, rejections, and level of skill in the art

The rejections are based on the following prior art:

Grants et al. (Grants)	4,281,392	July 28, 1981
Kinoshita	5,113,369	May 12, 1992
Bowater et al. (Bowater)	5,301,278	Apr. 5, 1994 (filed Apr. 23, 1992)

Claims 1-4 stand rejected under § 103 for obviousness over Bowater in view of Grants. Claims 11 and 12 stand rejected under § 103 for obviousness over Bowater in view of Grants and Kinoshita.

The level of skill in the art is represented by the references. See In re Oelrich, 579 F.2d 86, 91, 198 USPQ 210, 214 (CCPA 1978) ("the PTO usually must evaluate both the scope and content of the prior art and the level of ordinary skill solely on the cold words of the literature"); In re GPAC Inc.,

57 F.3d 1573, 1579, 35 USPQ2d 1116, 1121 (Fed. Cir. 1995) (Board did not err in adopting the approach that the level of skill in the art was best determined by the references of record).

D. Appellants' burden of persuasion on appeal

In re Rouffet, 149 F.3d 1350, 1355, 47 USPQ2d 1453, 1455 (Fed. Cir. 1998), explains that

> [t]o reject claims in an application under section 103, an examiner must show an unrebutted prima facie case of obviousness. See In re Deuel, 51 F.3d 1552, 1557, 34 USPQ2d 1210, 1214 (Fed. Cir. 1995). In the absence of a proper prima facie case of obviousness, an applicant who complies with the other statutory requirements is entitled to a patent. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). On appeal to the Board, an applicant can overcome a rejection by showing insuffi- cient evidence of prima facie obviousness or by rebutting the prima facie case with evidence of secondary indicia of nonobvious- ness. See id.

E. The § 103 rejection of claims 1-4 based on Bowater and Grants

Claim 1 is directed to the technique of obtaining information about an external memory by sampling, at a predetermined time in a memory cycle, protocol signals provided by the memory.

Bowater discloses a dynamic memory controller operable with dynamic RAMs having a wide range of operating characteristics (col. 3, lines 9-11). Bowater explains (col. 4, lines 33-44) that his invention

> allows the speed parameters and style to be individually programmed based on two factors:
>
> 1. The bank of memory being accessed--several different banks of memory can be controlled by the same memory controller (some could be video RAM, some could be static column mode, etc.), and the memory accesses are modified for each bank in order to maintain optimum performance.
>
> 2. The source of the memory request--different sources of the request can also influence the access (such as requiring extra data hold time which effectively increases the CAS access time).

Referring to Figure 3, a memory controller 110 for controlling DRAM banks 120 and 121 and VRAM banks 122 and 123 is responsive to memory requests generated by microprocessor 100 and other sources 101-104. Referring to Figure 4, which shows the internal components of memory controller 110, these memory requests are applied to request prioritization and address selection logic 200. The types of memory to be controlled are provided to state machine configuration

registers 230 by the microprocessor: "The registers 230 respond to the signal inputs from microprocessor 100 which are indicative of the source of the memory request and the type of memory bank accessed, to change the contents of the registers" (col. 8, lines 26-29). The control store 240 responds to the contents of the register 230 to change the duration of the cycle time of the control signals applied to the selected memory bank (col. 8, lines 29-32). Specifically, the access time and precharge time of RAS and CAS are modified (col. 8, lines 32-34). The examiner concedes that "Bowater does not teach auto-detecting the type of memory by polling data from a predetermined feedback line of the memory module (or memory port)" (Answer at 5). For this teaching the examiner relies on Grants.

Grants discloses a memory control circuit which "includes a decoder circuit which connects to selected leads in the machine's address bus and which connects to size feedback lines that connect to the memory modules and which indicate to the decoder circuit the size of the memory modules being used" (col. 1, lines 43-49). Referring to Figure 2A,

memory modules 30-33 include terminals 58-61 which are connected to ground within the module if the memory size is 1K and are left unconnected if the memory size is 4K (col. 6, lines 5-12). These terminals are connected via feedback lines 53-56 to the four least significant address terminals (A-D) of decoder PROM 52, of which the four most significant address terminals (E-H) receive address signals AB10-AB13 held in address latch 48 (col. 5, line 61, to col. 6, line 1). The four PROM output terminals 65 are connected as inputs to respective gates 66-69, which are "commonly connected to a STROBE control line 70 which is driven to a logic high voltage after an address is clocked into the address latches 45-48" (col. 6, lines 21-29). The decoder PROM 52 is programmed to generate a logic high voltage at one of the output terminals 65 when it is addressed, with the result that one of the four memory modules 30-33 is enabled through its chip select (CS) and strobe (STR) terminals when an address within the 16K address range of the memory circuit appears on the address bus 3 (col. 6, lines 30-36). The particular memory enabled is

determined by address bus leads AB10-AB13 and the state of the size feedback lines 53-56 (col. 6, lines 36-39).

The examiner contends that it would have been obvious "to modify Bowater's memory controller with Grants' teaching for providing a circuit for auto-detecting [the] type of memory module used in the system because it would have further increased the flexibility and versatility of Bowater's memory controller" (Answer at 6). Appellants argue that Bowater thus modified will not satisfy claim 1's requirement for a "static decoder . . . for sampling inputs on said memory protocol input lines at a pre- determined time in a memory cycle." Specifically, appellants argue that Grants fails to disclose (a) taking any samples of memory protocol input lines and (b) performing such sampling "at a predetermined time in a memory cycle." Regarding point (a), appellants submit that Grants

> fails to make obvious [the claimed] sampling of the memory protocol input lines. Note in Grants et al that the signals from the memory size feedback lines 58 to 61 of the memory modules 51 are continuously supplied to decoder PROM 52 via wiring in the circuit board. This

> negates any inference that these memory size feedback lines 58 to 61 are sampled at a predetermined time in a memory access cycle as recited in claim 1. [Brief at 13.]

The examiner responds that "by using the combination of address latches, gates and strobe signals, the decoder 52 indeed samples, reads, or obtains the memory size signals to generate other memory control signals during a memory cycle" (Answer at 10).

We agree with the examiner and further note that the artisan, when incorporating Grants' memory size auto-detect feature in Bowater's system, would realize that the memory module selection function provided by Grants' latch 48, PROM 52, and gates 66-69 are not needed in Bowater's system, in which that function is performed by memory controller 110. In other words, the artisan would appreciate that it is only necessary to provide each of Bowater's memory elements with means (e.g., a grounded or ungrounded terminal) for producing a signal representative of the memory size, which signal would then be sampled under the control of Bowater's microprocessor 100

(Fig. 3). We note that appel- lants, in responding to the now-withdrawn § 112 rejection, concede that

> the technique of sampling inputs at a predetermined time as recited in claims 1, 11, 19 and 28 is well known in the art. It is known in the art to capture the state of
>
> a particular input at a particular time for use. The Appellants respectfully submit that this technique is so well known in the art that it does not require further elaboration here. [Brief at 6.]

As for point (b), i.e., sampling the inputs "at a predetermined time in a memory cycle," appellants do not argue, and we do not believe, that the phrase "a memory cycle" must be construed to mean "every memory cycle." Thus, the limitation at issue, when broadly construed, is broad enough to read on sampling the memory size signals in Bowater as modified above during a single memory cycle. Appellants have not explained why it would have been unobvious from Grants, which discloses sampling during every memory cycle, to sample the memory size inputs at a predetermined time in at least one memory cycle.

The § 103 rejection of claim 1 is therefore affirmed, as is the § 103 rejection of dependent claims 2-4, which are not separately argued.

F. The § 103 rejection of claims 11 and 12 based on Bowater, Grants, and Kinoshita

Claim 11 is directed to the technique of bus size recognition and selection.

Kinoshita discloses "a simple, low-cost personal computer having a 32-bit microprocessor compatible with existing

16-bit personal computer software" (col. 1, lines 35-38). Referring to Figure 1, peripheral LSIs identified as VLSIA 3 and VLSIB 4 are arranged between MPU (Micro Processing Unit) 1 and various peripheral devices (col. 2, lines 18-26). VLSIA controls and interfaces between the MPU bus and other devices, such as external devices and memories (col. 2, lines 36-38). VLSIA 3 includes a latch 301 and a bus width converter 302, shown in Figure 2 (col. 5, lines 14-15 and 31-32). As shown in Figure 3, latch 301 includes drivers/receivers 301_1, 301_3, and 301_4 for receiving bit groups 16-31, 8-15, and 0-7,

respectively, from MPU 1 (col. 5, lines 32-36). The outputs of these drivers/ receivers are connected to bus width converter 302, which includes drivers/receivers 302_1, 302_3, 302_4, and 302_5 for outputting 16-bit or 8-bit data (col. 5, lines 39-51). The examiner contends it would have been obvious

> to utilize Kinoshita's bus convertor in the combined Bowater and Grants's memory interface controller because it would have further increased the utility of the memory controller by enabling the processor to interface with various memory devices having different data widths. [Answer at 8.]

Appellants argue that the teachings of the references thus combined will not satisfy claim 11's requirement for "an external port having . . . a plurality of bus size input lines" and a "decoding circuit . . . for sampling input on said bus size input lines." We agree with this argument, which has not been addressed by the examiner. Kinoshita does not disclose or suggest automatically determining bus size by sampling input signals from an external port or a device coupled thereto. Nor is this suggestion found in Kinoshita considered with

Bowater and Grants. Accordingly, we are reversing the § 103 rejection of claim 11 and its dependent claim 12.

No time period for taking any subsequent action in con- nection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

JOHN C. MARTIN Administrative Patent Judge	)	
MICHAEL R. FLEMING Administrative Patent Judge	)	BOARD OF APPEALS AND INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)	

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