

The opinion in support of the decision being entered today is **not** binding precedent of the Board.

Paper No. 14

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RICHARD J. DISCHLER, JIM KLUMPP,
and REINHARD SCHUMANN

Appeal No. 1997-3792
Application No. 08/321,334¹

ON BRIEF

Before THOMAS, MARTIN, and BARRETT, Administrative Patent Judges.

MARTIN, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-3, 5, and 7-13. Claim 6 has been canceled and claim 4 stands objected to for depending on a rejected claim. We reverse all of the

¹ Application filed October 11, 1994.

rejections and enter a new ground of rejection of claims 1-3, 5, and 7-10 pursuant to 37 CFR § 1.196(b).

A. The invention

The invention relates to circuitry for controlling the clock speed and/or power supply voltage of a microprocessor in order to reduce its power consumption while keeping its temperature within acceptable limits. Referring to Figure 1, a thermistor 21 adjacent to heat sink 22 delivers a signal representing the temperature of microprocessor (CPU) 13 (Spec. at 11, lines 6-18). This temperature signal is applied to microcontroller 20, which uses the heat management algorithm depicted in Figures 5A and 5B to calculate the maximum allowable clock frequency of the CPU (Spec. at 17, lines 15-25). Specifically, steps 82-87 of this algorithm (Fig. 5A) calculate an "expected" (i.e., future) temperature T_{k+2} that is compared in step 88 (Fig. 5B) to T_{MAX} , the maximum allowable temperature for the CPU (Spec. at 18, line 18 to p. 19, line 18). Alternatively, the algorithm can compare the current temperature to T_{MAX} (Spec. at 18, lines 12-17). Depending on the result of the comparison and whether TURBO operation has been asserted (step 91), the algorithm may or

may not obtain a new maximum clock frequency value from one of three frequency tables (steps 89, 94, and 92). If the TURBO option has been asserted (step 91 in Fig. 5B), the supply voltage to the microprocessor is increased to the required value (step 93), which can be accomplished using the circuitry of Figure 3 (Spec. at 14, line 8 to p. 16, line 2). Step 95 represents the act of storing a newly calculated maximum clock frequency in register 34b (Fig. 2), which stores either the maximum rated clock frequency of the CPU or the new maximum clock frequency obtained using the algorithm (Spec. at 13, lines 15-21). Register 34a stores a minimum clock frequency value representing the lowest clock frequency capable of maintaining refresh operations (Spec. at 13, lines 8-15). Multiplexer 36 is responsive (via state device 31a) to an IDLE/BUSY bit in control and status register 31 to cause the multiplexer to select the maximum clock frequency value during BUSY periods and the minimum clock frequency value during IDLE periods (Spec. at 12, line 21 to p. 13, lines 2-5). The selected value is applied to a phase lock loop (PLL) circuit 38, which produces a clock signal having the specified minimum or maximum frequency.

Figure 6 shows a microcontroller thread which determines whether the current clock frequency is lower than the lowest frequency (F_{rv}) at which the CPU can operate with a reduced supply voltage and, if the answer is yes, asserts a signal REDUCE_V in order to reduce the supply voltage to the CPU (Spec. at 20, line 22 to p. 21, line 8).

Figure 7 shows an alternative heat management algorithm in the form of a table in which the temperature or temperature range being is used as an index to access values representing the required clock frequency, supply voltage and fan setting (Spec. at 21, lines 9-20).

B. The claims

Claims 1 and 11, the only independent claims on appeal, read as follows:

1. A computer system comprising:

a microprocessor;

means for generating a clock signal, said means including means responsive to a control signal for selecting a maximum clock signal frequency value; and

means for adjusting the maximum clock signal frequency value in accordance with idle and busy operating conditions of the microprocessor.

11. A computer system comprising:

a microprocessor;

means for varying a magnitude of a supply voltage fed to the microprocessor in accordance with the temperature of the microprocessor and the operating frequency of the microprocessor.

C. The references and rejections

The references relied on by the examiner are:

Perry et al. (Perry)	5,142,684	Aug. 25, 1992
Georgiou et al. (Georgiou)	5,189,314	Feb. 23, 1993
Kenny et al. (Kenny)	5,287,292	Feb. 15, 1994
Lin	5,452,401	Sep. 19, 1995
		(filed Mar. 31, 1992)

Claims 1-3 stand rejected under § 102(e) as anticipated by Kenny.

Claims 5 and 7-10 stand rejected under § 103 for obviousness over Kenny in view of Perry.

Claim 11 stands rejected under § 102(e) as anticipated by Lin.

Claim 12 stands rejected under § 103 for obviousness over Lin in view of Perry.

Claim 13 stands rejected under § 103 for obviousness over Lin in view of Perry and Georgiou.

D. New grounds of rejection under 35 U.S.C. § 112

The following new grounds of rejection under 35 U.S.C. § 112 are hereby entered pursuant to our authority under 37 CFR § 1.196(b).

1. Lack of written description support (§ 112, ¶ 1)

Comparing claim 1 to appellants' disclosure, the claimed "microprocessor" reads on CPU 13 of Figure 1; the claimed "means for generating a clock signal, said means including means responsive to a control signal for selecting a maximum clock signal frequency value" reads on at least register 34b, multiplexer 36, and phase lock loop circuit 38 of Figure 2. The multiplexer is responsive to the IDLE/BUSY signal (the claimed "control signal") to select, during BUSY intervals, the maximum clock signal frequency value stored in register 34b for application to the input of the phase lock loop circuit, which generates the corresponding maximum frequency clock signal.

It would appear that the claimed "means for adjusting the maximum clock signal frequency value in accordance with idle and busy operating conditions of the microprocessor" is intended to be read on adjustment of the maximum clock

frequency value in accordance with the temperature (current or expected) of the microprocessor, i.e., in accordance with the heat management algorithm shown in Figures 5A and 5B or in Figure 7. The fact that it is the maximum clock signal frequency value which is being adjusted implies that the adjustment is based on the temperature of the CPU during only the busy periods, when the CPU is being operated at the maximum clock frequency and may experience an increase in temperature. Therefore, the claim is inaccurate to state that the maximum clock frequency value is adjusted "in accordance with idle and busy operating conditions of the microprocessor" (emphasis added). This "idle and busy" language, which was added to claim 1 by amendment,² lacks written description support in the specification (including claims) as filed, which more generally calls for adjusting the maximum clock frequency value "in accordance with operating conditions of the central processor" (Abstract; Spec. at 6, lines 7-9; Spec. at 7, lines 18-21) or "in accordance with the operating conditions which the microprocessor is being exposed to" (Spec. at 12, lines 6-10).

² Amendment received April 25, 1996 (paper No. 4).

For the foregoing reasons, we are rejecting claim 1 and its dependent claims 2-5 and 7-10 (including originally objected-to claim 4) under 35 U.S.C. § 112, first paragraph, as lacking written description support in the application as originally filed.

2. Indefiniteness (§ 112, ¶ 2)

We are also rejecting claim 1 under § 112, ¶ 2 as indefinite because the absence of any reference to a "minimum clock signal frequency value" in that claim makes the meaning of the recited "maximum clock signal frequency value" unclear. Maximum in comparison to what? Would the claimed "means . . . for selecting a maximum clock signal frequency value" read on a circuit that selects between a given clock signal frequency and no clock frequency, i.e., gating a clock signal on and off?

Unlike claim 4, dependent claims 2, 3, 5, and 7-10 do not remove this ambiguity and therefore are rejected on the same ground. (We note that the expression "the minimum . . . clock frequency" (emphasis added) in claim 8 lacks a clear antecedent.)

**E. The examiner's § 102 and § 103
rejections of claims 1-3, 5, and 7-10**

Although we are of the opinion that the term "maximum clock frequency" in claims 1-3, 5, and 7-10 renders those claims indefinite, that indefiniteness is not such as to preclude us from considering the merits of the examiner's prior art rejections and concluding that they cannot be sustained.

Kenny's first embodiment (Fig. 1) is responsive to a status line 101 (CPUCLKHI) which is "hot" or one when the CPU clock frequency is fast (e.g., at 33 MHZ) and is "cool" or zero when the CPU clock is slow (e.g., 1 MHZ) (col. 5, lines 46-49). The status line is periodically sampled by flip-flop 105 in response to a sampling clock signal on line 104 to produce on line 110 a signal (SMPLHOT) indicating whether the CPU is "hot" or "cool" (col. 5, lines 52-57). The "hot" and "cool" signals are accumulated and averaged in an up/down counter 108, which increments or decrements once for every sampling of CPU speed (col. 5, lines 58-63). If the count reaches a binary 1000 (i.e., decimal 8), a FORCESLOW signal is issued to reduce the CPU clock speed (col. 5, line 64 to col. 6, line 2). After the threshold value is reached, the

embodiment of the invention in FIG. 1 maintains no more than one time interval of the CPU running "hot" for every interval of the CPU running "cool"; thus, the ratio of time running "hot" to time running "cool" is approximately equal to or less than one (col. 6, lines 8-14). This is described as a power use ratio of 50% (col. 6, line 53).

The embodiment of Figures 2a and 2b is responsive, via multiplexer 229, to status lines representing CPU bus speed (CPUCLKHI) and bus activity (BUSACTV) (col. 7, lines 12-22). Line BUSACTV is high when there is bus activity (col. 7, line 68 to col. 8, line 1).

The Figure 4 embodiment includes a heat generation sensor 402 (responsive to status lines 401), an excess heat counter 405, and a cooling trigger 407 (col. 9, lines 8-31). When the counter reaches a count indicating that the circuit to be protected has reached a particular temperature, cooling trigger 407 issues a "cooling trigger" signal on line 408 to force the circuit that is being monitored to cool, such as by "reduc[ing] the clock speed of the circuit" (col. 9, lines 31-35).

The Figure 5 embodiment is responsive to a temperature monitor 501 rather than a status line.

In each of the foregoing embodiments, the output trigger signal generated in response to the counter determines (i.e., selects) whether the CPU clock will be changed to the lower speed or permitted to continue operatm l's requirement for "means . . . for selecting a maximum clock ion at the higher speed. Thus, each embodiment satisfies claisignal frequency value" (emphasis aded). More particularly, in the embodiments of Figures 1, 2a-2b, and 4 the CPU speed is selected in response to status signals not representing temperature, whereas in the Figure 5 embodiment the CPU speed is selected in response to temperature. However, none of these embodiments includes apparatus satisfying claim 1's additional requirement for "means for adjusting the maximum clock signal frequency value in accordance with . . . operating conditions of the microprocessor" (emphasis added). The examiner's position appears to be that this limitation reads on the same circuitry that performs the selection function, i.e., the circuitry which determines whether the clock should be slowed or permitted to continue to run at high speed. We do not

agree. In our view, the claim requires that the selected "maximum clock signal frequency value" be adjusted either before or after it is selected, a function which is not performed in any of Kenny's embodiments.³ For this reason, the rejection of claim 1 and dependent claims 2 and 3 for anticipation by Kenny is reversed.

We also agree with appellants that Kenny fails to disclose means for calculating an expected (i.e., future) temperature, as required by claim 2. The Figure 5 embodiment, the only embodiment responsive to temperature, responds to current temperature without making calculations of an expected temperature. The temperature calculations discussed in Kenny at column 6, lines 34-61, on which the examiner relies, are

³ Consequently, we do not reach appellants' argument that Kenny fails to disclose adjusting the maximum clock signal frequency in accordance with idle and busy operating conditions of the microprocessor. However, we will address the examiner's characterization of Kenny's low speed (e.g., 1 MHZ) clock signal as an "idle" operating condition (Answer at 3). "[I]dle time" is defined in the TechEncyclopedia as "[t]he duration of time a device is in an idle state, which means that it is operational, but not being used. See <http://www.techweb.com/encyclopedia/defineterm?term=IDLETIME&exact=> (copy enclosed). Is the examiner's position that Kenny's CPU is inherently (i.e, necessarily) inactive during at least part of the time it is being operated at the lower clock speed?

performed by the operator, not by the disclosed apparatus.

As the examiner has not explained how the foregoing deficiency with respect to claim 1 is remedied by Perry, the § 103 rejection of claims 5 and 7-10, which depend on claim 1, based on Kenny in view of Perry is also reversed.

F. The examiner's § 102 and § 103 rejections of claims 11-13

Claim 11, rejected for anticipation by Lin, recites "means for varying a magnitude of a supply voltage fed to the microprocessor in accordance with the temperature of the microprocessor and the operating frequency of the microprocessor." Comparing this claim to appellants' disclosure, raising the supply voltage in response to temperature corresponds to steps 82-88 and 90-92 of Figs. 5A and 5B, while control of the supply voltage in response to frequency is depicted by steps 92, 94, and 96 of Figure 6.

In our view, the claim when given its broadest reasonable construction requires that the supply voltage be varied in response to the temperature (actual or expected) and the operating frequency, which does not occur in Lin. Lin reduces power consumption by turning on and off the functional units of the microelectronic device in accordance with the

requirements of the program being executed (col. 3, lines 50-54). Specifically, a logic unit evaluates (e.g., decodes or monitors) the machine code during execution, and based on utilization information provided by the compiler, determines at each step in the execution of the computer program which functional units are needed for execution, and therefore should be turned on or off (col. 4, lines 14-20). When the functional units are CMOS circuits, which consume no power when they are not changing state (col. 4, lines 63-64), a functional unit can be turned off by (1) stopping application of the clock signal to the functional unit or (2) stopping the inputs of the functional unit from being changed (col. 4, lines 53-58). Coupling/decoupling of a power supply bus is also envisioned by adding controllable power switches between the supply voltage V_{DD} and the functional units (col. 7, lines 34-35). Assuming for the sake of argument that Lin discloses turning off a given functional unit by disconnecting both its power supply voltage and its clock signal (which can be considered to be changing the clock frequency to zero), the power supply voltage is not being turned off in accordance with (i.e., in response to) the operating frequency, as

required by the claim. Rather, both are being turned off in response to other control signals. The § 102 rejection of claim 11 over Lin is therefore reversed.

As the examiner has not explained how the foregoing deficiency is remedied by Perry, which is relied on together with Lin to reject dependent claim 12, or by Georgiou, which is relied on with Lin and Perry to reject dependent claim 13, the § 103 rejection of those claims is reversed.

This decision contains a new ground of rejection pursuant to 37 CFR § 1.196(b) (amended effective Dec. 1, 1997, by final rule notice, 62 Fed. Reg. 53,131, 53,197 (Oct. 10, 1997), 1203 Off. Gaz. Pat. & Trademark Office 63, 122 (Oct. 21, 1997)).

37 CFR

§ 1.196(b) provides that, "A new rejection shall not be considered final for purposes of judicial review."

37 CFR § 1.196(b) also provides that the appellants, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of proceedings (§ 1.197(c)) as to the rejected claims:

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(1) Submit an appropriate amendment of the claims so rejected or a showing of facts relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the application will be remanded to the examiner. . . .

(2) Request that the application be reheard under § 1.197(b) by the Board of Patent Appeals and Interferences upon the same record. . . .

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

REVERSED; 1.196(b)

JAMES D. THOMAS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
JOHN C. MARTIN)	
Administrative Patent Judge)	APPEALS AND
)	
)	INTERFERENCES
)	
LEE E. BARRETT)	
Administrative Patent Judge)	

JCM:tdl

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Patent Law Group
Digital Equipment Corporation
111 Powdermill Road, MS02-3/G3
Maynard, MA 01754-1499