

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JOHANNES BIRZER

Appeal No. 1997-3743
Application 08/419,166

ON BRIEF

Before THOMAS, KRASS and DIXON, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal from the examiner's final rejection of claims 1 through 4 and 9. Since the examiner has allowed claims 1 through 4 at page 2 of the answer, the only claim

that remains on appeal is claim 9.

Claim 9 is reproduced below:

9. A system for communicating data between a peripheral unit of a modular programmable controller having at least one

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central processing unit and a unit external to the modular programmable controller, the system comprising:

a first bus via which the at least one central processing unit and the peripheral unit communicate; and

a busable programming interface located on the central processing unit, the external unit being coupled to the busable programming interface;

wherein communication between the peripheral unit and the external unit takes place by means of differential signal transmission via the busable programming interface and a second bus arranged within the modular programmable controller.

The following references are relied on by the examiner:

Mathews et al. (Mathews)	5,225,974	July
6, 1993		
Nakayama	5,349,679	Sep. 20,
1994		
		(filed Aug. 27, 1991)

Claim 9 stands rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon Mathews in view of Nakayama.

Rather than repeat the positions of the appellant and the examiner, reference is made to the brief and the answer for the respective details thereof.

OPINION

Generally for the reasons set forth by the examiner in the answer with respect to his analysis of Mathews, we sustain the rejection. Inasmuch as we are in agreement with appellant's

observation at the top of page 6 of the brief that with respect to the claimed invention on appeal, no interface is switched off or bypassed, the examiner's reliance upon Nakayama is lessened. Therefore, we consider this reference to be cumulative to the teachings already indicated in Mathews.

Appellant's view of Mathews and his teachings is incomplete. Moreover, appellant appears to attempt to persuade us of the patentability of claim 9 on appeal based upon the numerous features disclosed but unclaimed. Page 4 of the answer details the examiner's view that the use of differential serial buses was well known in the art even though the examiner and we recognize that there is no explicit teaching of this feature in Mathews. Appellant does not contest this observation of the examiner that such a communication approach was well-known in the art and, in fact, appellant's own disclosed invention of the interfacing standard RS-485, on which the claimed feature appears to be based, is based upon a well-known industry standard. Differential signaling is nothing more than the digital signal version of a well-known balanced transmission line approach utilizing two conductors such as a twisted pair to form a complete circuit,

where the binary value depends on the direction of the voltage difference between the two conductors.

In figures 1 and 2 of Mathews, the UART 28 is a serial communication device connecting the program terminal 11 to the primary rack 12 and specifically to the first communication processor 21 in a serial mode. Similarly, the first network interface 29 in Figure 2 connects the local area network 17 to this first communication processor 21 in a serial mode. The same may be said of the second network interface 76 to interconnect the various input/output racks 14 on bus 15. Each of these devices clearly converts external serial information on buses 13, 15 and 17 to internally busable parallel information for the various internal parallel buses and vice-versa for transmission on the various busses noted. These features are generally discussed at column 3, lines 29 through 41; column 4, lines 10 through 30; and column 6, lines 13 through 16. At least with respect to the UART 28, there is an explicit statement in Mathews that several commercially available devices may comprise this unit, and such is similarly implied for the first network interface 29 and the second network interface 76 since these devices have no additional explicit teaching of their details in

Mathews, thus necessitating reliance upon what was known in the art.

According to the examiner's rejection, the second bus is bus 13 connecting the programming terminal 11 to the primary rack 12 in Figure 1 by means of UART 28 in Figure 2. Column 4, lines 19 through 23 indicate that the port UART 28 may be coupled to other types of serial devices for the exchange of data with the entire processor module 20 shown in all of Figure 2.

Claim 9 only recites a peripheral unit and an external unit that appear to be indirectly interconnected. In contrast to the assertion at page 5 of the brief there are no claimed separate peripheral interfaces and a communication interface in claim 9 on appeal. Only "a busable programming interface" is recited. Broadly speaking, according to the examiner's rationale and a reliance upon Mathews, it appears that the first communication processor 21 as well as the general purpose processor 60 along with the second communication processor 70 provide clear indications in Figure 2 of this busable programming interface in this reference notwithstanding the additional capability of input/output communications through the I/O rack interface circuit 38 further shown in detail in Figure 4, which in turn provides two separate programmable processing elements for

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intercommunication of various process sensed and controlled devices by means of the backplane of the rack 12.

In view of the foregoing, the decision of the examiner rejecting claim 9 on appeal is affirmed.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

	James D. Thomas)	
	Administrative Patent Judge)	
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	Errol A. Krass)	BOARD OF
PATENT	Administrative Patent Judge)	APPEALS AND
)	INTERFERENCES
)	
	Joseph L. Dixon)	
	Administrative Patent Judge)	

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