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The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KIM C. HARDEE

Appeal No. 1997-3436
Application No. 08/432,884¹

ON BRIEF

Before KRASS, BARRETT, and BARRY, Administrative Patent Judges.
BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the final rejection of claims 14, 18, and 31-44. We reverse.

BACKGROUND

¹ The application was filed on May 2, 1995. It is a divisional of Application Serial No. 07/976,312, which was filed on November 12, 1992 and is now abandoned.

The invention at issue in this appeal is a sense amplifier for use in an integrated circuit (IC) memory. An IC memory includes many memory cells, which are arranged in rows and columns. A column is a collection of memory cells along a bit line pair. Each column is connected to a sense amplifier. The sense amplifier senses the effect a memory cell has on the bit line pair and amplifies a signal for reading data from the memory cell. In addition, the sense amplifier drives the bit line pair for writing data into the memory cell.

When conventional sense amplifiers are employed in large memories, the amplifiers work inefficiently and slowly, prolong access time, suffer pattern sensitivities, and are unstable. The invention aims to overcome these problems. In particular, the inventive sense amplifier includes a latch circuit coupled to a pair of bit lines of an IC memory and a pair of local data write driver circuits coupled to the latch circuit. The local data write driver circuits are coupled to a data write control signal so that a power supply voltage may be selectively applied, via the driver circuits, to the latch circuit and to a corresponding bit line. A pass transistor is

Rather than repeat the arguments of the appellant or examiner in toto, we refer the reader to the briefs and answer for the respective details thereof.

OPINION

In reaching our decision in this appeal, we considered the subject matter on appeal and the rejection and evidence advanced by the examiner. Furthermore, we duly considered the arguments of the appellant and examiner. After considering the totality of the record, we are persuaded that the examiner erred in rejecting claims 14, 18, and 31-44. Accordingly, we reverse.

We begin by noting the following principles from Rowe v. Dror, 112 F.3d 473, 478, 42 USPQ2d 1550, 1553 (Fed. Cir. 1997).

A prior art reference anticipates a claim only if the reference discloses, either expressly or inherently, every limitation of the claim. See Verdegaal Bros., Inc. v. Union Oil Co., 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "[A]bsence from the reference of any claimed element negates anticipation." Kloster Speedsteel AB v. Crucible, Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

With these principles in mind, we consider the appellant's argument and the examiner's reply.

The appellant argues, "the elements of Claims 14 and 40 requiring a local data write driver circuit (Claim 14) or first and second local data write driver circuits (Claim 40) are neither disclosed nor suggested by Ohsawa." (Appeal Br. at 21.) The examiner replies, "Ohsawa clearly shows the local data write driver circuits 14-15 because the local data write driver circuits 14-15 of Ohsawa are ON/OFF controlled in response to a signal from the signal line WRT and hence transmit the information on the data input/output lines DQ-DQ to the bit lines BL-BL (see fig. 3 and col. 4, lines 1-53)." (Examiner's Answer at 4.)

"[T]he main purpose of the examination, to which every application is subjected, is to try to make sure that what each claim defines is patentable. [T]he name of the game is the claim'" In re Hiniker Co., 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998) (quoting Giles S. Rich, The Extent of the Protection and Interpretation of

Claims--American Perspectives, 21 Int'l Rev. Indus. Prop. & Copyright L. 497, 499, 501 (1990)). Here, claims 14, 18, and 31-39 each specify in pertinent part the following limitations: "a local data write driver circuit coupled to receive write data during a write operation at a gate electrode of a transistor in said data write driver circuit" Similarly, claims 40-44 each specify in pertinent part the following limitations: "first and second local data write driver circuits, each being configured to receive a respective data signal at a respective gate electrode of first write driver transistors in said first and second local data write driver circuits" Accordingly, the claims each require receiving data at a gate electrode of a transistor of a write driver circuit.

The examiner fails to show a disclosure of the claimed limitations in the prior art. "The Patent Office has the initial duty of supplying the factual basis for its rejection. It may not . . . resort to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies in its factual basis."

In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967).

Although Ohsawa discloses receiving a signal from line WRT at respective gate electrodes of data write n-channel MOS transistors 14 and 15, col. 4, ll. 23-28, the examiner does not show that the signal is a data signal or that the transistors are write driver circuits. We address these defects seriatim.

Rather than being a data signal, the reference suggests that the signal from line WRT is a control signal. The examiner admits, "circuits 14-15 of Ohsawa are ON/OFF controlled in response to a signal from the signal line WRT" (Examiner's Answer at 4.) For its part, the reference teaches, "[t]he gates of the data write transistors 14 and 15 are connected to a data write **control** line WRT, and the transistors 14 and 15 are simultaneously ON/OFF-controlled in response to a signal from the signal line WRT." Col. 4, ll. 26-30 (emphasis added). In summary, rather than specifying data, the WRT signal controls whether transistors 14 and 15

are on or off. Furthermore, the figure cited by the examiner shows that neither of the data input/output lines is connected to the respective gates of the transistors 14 and 15. Fig. 3. In other words, the gates of the transistors are not shown to receive any data signals.

Data write n-channel MOS transistors 14 and 15 possibly could be interpreted as being write driver circuits; however, the transistors could also be interpreted as pass transistors. The examiner does not contest that appellant's definition that "[a] pass transistor simply (selectively) passes a voltage from one node to another. On the other hand, a driver circuit drives an output high or low." (Appeal Br. at 20.) The examiner's assertion that transistors 14 and 15 "transmit the information on the data input/output lines DQ-DQ to the bit lines BL-BL," (Examiner's Answer at 4), is consistent with the appellant's definition of a pass transistor, which would mean that transistors 14 and 15 are pass transistors rather than write driver circuits.

In view of the reference's teachings and showings, the appellant's definition, and the examiner's assertion, the examiner's interpretation amounts to speculation or an unfounded assumption. Accordingly, we are not persuaded that the reference discloses the claimed limitations of "a local data write driver circuit coupled to receive write data during a write operation at a gate electrode of a transistor in said data write driver circuit" or "first and second local data write driver circuits, each being configured to receive a respective data signal at a respective gate electrode of first write driver transistors in said first and second local data write driver circuits" The absence of this disclosure negates anticipation. Therefore, we reverse the rejection of claims 14, 18, and 31-44 as anticipated by Oshawa.

CONCLUSION

To summarize, the examiner's rejection of claims 14, 18, and 31-44 under 35 U.S.C. § 102(e) is reversed.

REVERSED

ERROL A. KRASS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
LEE E. BARRETT)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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