

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte KENNETH P. PARKER and STIG ORESJO

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Appeal No. 1997-3133  
Application No. 08/370,076

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HEARD: April 5, 2000

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Before KRASS, RUGGIERO, and DIXON, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 13 through 28, all of the claims remaining in the application.

The invention pertains to boundary scan testing and, in particular, is directed to a post-mission test method for assuring the integrity of the boundary scan test. The integrity of the scan path is checked after test execution but before test diagnosis. By comparing the bit length of the scan path before execution of the mission test with the bit length of the scan path after test execution, the integrity of the scan path is checked. If the bit length of the scan path has changed, the mission test is known to be invalid and a test technician's time is not wasted trying to diagnose and repair a circuit board, which may be working properly, because of erroneous test results.

Representative independent claim 13 is reproduced as follows:

13. A boundary scan testing method for performing a mission test on a circuit under test formed by a plurality of interconnected integrated circuit (IC) chips, each chip having internal logic and a boundary scan circuit, wherein the plurality of boundary scan circuits are interconnected to form a scan path, and confirming the integrity of the mission test after the mission test has been performed, comprising the steps of:

executing the mission test on the circuit under test, wherein the scan path has a pre-test configuration;



determination of a post-test scan path configuration and the comparison thereof with a pre-test scan path configuration, that Hassan suggests these claim limitations in the disclosure of loading test vectors, shifting responses for detection of faults and comparing with an expected response.

Hassan is clearly directed to the type of system referred to by appellants in the background of the specification wherein interconnects are tested and diagnosed using boundary scan architecture. However, appellants' improvement thereover, as explained in the specification and set forth in the instant claims, is to confirm the integrity of a mission test performed on a circuit by executing the mission test on a circuit wherein the scan path has a pre-test configuration and then determining, after performance of the mission test, a post-test configuration of the scan path. The result of a comparison of the pre- and post-test configurations of the scan path determines whether the mission test was valid. Hassan neither discloses nor suggests such a scheme for determining the integrity of a mission test. Conventional testing techniques, of which Hassan is representative, assume that the post-test configuration of the scan path is the same as the pre-test

configuration. Any change in the scan path configuration will go unnoticed in Hassan and lead to erroneous results. While Hassan discloses test generation and diagnosis for verifying the interconnections of integrated circuits, there is no suggestion of determining a post-test configuration of the scan path and certainly no suggestion of comparing it with a pre-test configuration of the scan path.

Independent claim 18 recites, more specifically, that there is a determination of the actual bit length of the scan path in the post-test configuration. While the examiner does not explain, with any degree of specificity, the significance of Parker or how or why it is being applied, ostensibly, the examiner relies on Parker for the determination of actual bit length of a scan path. Appellants point to Figure 5 of Parker where a diagnosis step immediately follows a "stop testing" step. Accordingly, it appears reasonable that Parker performs no action between stopping the test and diagnosing any faults, unlike the instant claimed invention wherein a shift in signature pattern through the scan path occurs in a post-test configuration in order to determine the actual bit length of the scan path in the post-test configuration. The examiner's

response does not address this issue of the Parker disclosure but, instead, contends that "it is the examiner's position that Hassan's counting number of '1's from the shifted out response is applicable to the claimed 'determination of the actual bit length of the scan chain'" [answer-page 6]. So, now it appears that Parker is not used by the examiner for such a showing. It is unclear to us what role, if any, Parker plays in the examiner's rejection. In any event, we disagree with the examiner's assessment that Hassan's counting of a number of 1's from the shifted out response is equivalent or analogous to the claimed determination of "an actual bit length of the scan path in said post-test configuration" because Hassan does not appear to be interested at all in determining the bit length of the scan path. Certainly, the examiner has made no prima facie showing that Hassan discloses or suggests the instant claimed subject matter.

Accordingly, the examiner's decision rejecting claims 13 through 28 under 35 U.S.C. 103 is reversed.

REVERSED

ERROL A. KRASS	)	
Administrative Patent Judge	)	
	)	
	)	
	)	
	)	BOARD OF PATENT
JOSEPH F. RUGGIERO	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
	)	
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	)	
JOSEPH L. DIXON	)	
Administrative Patent Judge	)	

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