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The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 28

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KIM C. HARDEE

Appeal No. 1997-2294
Application No. 08/284,183¹

ON BRIEF

Before KRASS, BARRETT, and BARRY, Administrative Patent Judges.
BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the rejection of claims 8, 9, 14-30, 32, 33, and 40-50. We reverse.

¹ The application was filed on August 2, 1994. It is a divisional of Application Serial No. 07/976,312, which was filed on November 12, 1992 and is now abandoned.

BACKGROUND

The invention at issue in this appeal is a sense amplifier for use in an integrated circuit (IC) memory. An IC memory includes many memory cells, which are arranged in rows and columns. A column is a collection of memory cells along a bit line pair. Each column is connected to a sense amplifier. The sense amplifier senses the effect a memory cell has on the bit line pair and amplifies a signal for reading data from the memory cell. In addition, the sense amplifier drives, i.e., controls, the bit line pair for writing data into the memory cell.

When conventional sense amplifiers are employed in large memories, the amplifiers work inefficiently and slowly, prolong access time, suffer pattern sensitivities, and are unstable. The invention aims to overcome these problems. In particular, the inventive sense amplifier includes a latch circuit coupled to a pair of bit lines of an IC memory and a pair of local data write driver circuits coupled to the latch circuit. The local data write driver circuits are coupled to

a data write control signal so that a power supply voltage may be selectively applied via the local data write driver circuits to the latch circuit and to a corresponding bit line. A pass transistor is coupled between the latch circuit and each of the local data write driver circuits to selectively apply an output signal from a local data driver circuit to the latch circuit and the corresponding bit line.

Claim 8, which is representative for our purposes, follows:

8. A sense amplifier arrangement for an integrated circuit memory comprising:
a latch circuit having internal nodes for coupling to a respective bit line pair;
a pair of pass transistors each coupled to a respective one of said internal nodes, the pass transistors having a control electrode coupled to receive a first control signal;
a pair of local data write driver circuits having respective control electrodes coupled to receive second write control signals for data write operations and to provide a pair of data write output signals, each local data write driver circuit being coupled to its corresponding pass transistor so that the pass transistor, when conductive, couples one of said output signals from the local data write driver circuit to the corresponding internal node of the latch circuit and to a corresponding bit line.

The reference relied on in rejecting the claims follows:

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McClure

5,267,197

Nov. 30, 1993
(Filed Dec. 13, 1990).

Claims 8, 9, 14-30, 32, 33, and 40-50 stand rejected under 35 U.S.C. § 102(e) as anticipated by McClure. Rather than repeat the arguments of the appellant or examiner in toto, we refer the reader to the briefs and answer for the respective details thereof.

OPINION

In reaching our decision in this appeal, we considered the subject matter on appeal and the rejection and evidence advanced by the examiner. Furthermore, we duly considered the arguments of the appellant and examiner. After considering the totality of the record, we are persuaded that the examiner erred in rejecting claims 8, 9, 14-30, 32, 33, and 40-50. Accordingly, we reverse.

We begin by recalling that a reference anticipates a claim only if it discloses expressly or inherently every limitation of the claim. Absence of any limitation from the reference negates anticipation. Rowe v. Dror, 112 F.3d 473, 478, 42 USPQ2d 1550, 1553 (Fed. Cir. 1997). With this in mind, we address the novelty of claims 8, 9, 14-21, 29, 30,

32, 33, and 50; the novelty of claims 22-28; and the novelty of claims 40-49.

Novelty of Claims 8, 9, 14-21, 29, 30, 32, 33, and 50

Regarding claims 8, 9, 14-21, 29, 30, 32, 33, and 50, the examiner asserts, "McClure shows all the limitations of the claimed sense amplifier arrangement in Figs. 1-10 (especially figs. 4-5), comprising a latch circuit 30" (Examiner's Answer at 3.) The appellant replies, "Memory cells 30 are undeniably the memory storage part of the claimed integrated circuit memory. They are not any part of a 'sense amplifier,' and no one of skill in the art would ever consider otherwise." (Reply Br. at 7.) We agree with the appellant.

Each of claims 8, 9, 14-21, 29, 30, 32, 33, and 50 specifies in pertinent part "[a] sense amplifier arrangement for an integrated circuit memory comprising: a latch circuit" In other words, each of the claims recites a latch circuit that is part of a sense amplifier.

The examiner errs in determining the content of the prior art. Although he refers to McClure's memory cells 30, the memory cells 30 are part of a column in a sub-array 12_n of an IC memory 1. Col. 8, ll. 10-13 (referring to Fig. 4). Figure 2 of the reference shows that McClure's sense/write circuits 13, i.e., the reference's sense amplifiers (SA0-SA7), are separate from the sub-array 12_n . Because McClure's memory cells 30 are not part of the reference's sense amplifiers 13, the examiner fails to show a teaching of the claimed "sense amplifier arrangement for an integrated circuit memory comprising: a latch circuit" The absence of this showing negates anticipation. Therefore, we reverse the rejection of claims 8, 9, 14-21, 29, 30, 32, 33, and 50 under 35 U.S.C. § 102(e). Next, we address the novelty of claims 22-28.

Novelty of Claims 22-28

Regarding claims 22-28, the examiner makes the following assertion.

McClure shows all the limitations of the claimed sense amplifier arrangement in Figs. 1-10 (especially figs. 4-5), comprising a latch circuit

30 coupled directly or indirectly to a pair of corresponding bit lines BL-BL-; first and second pass transistors 36p-36n; first and second local data write driver circuits WRSEL, 38j,54T-57T, 59T-60T, 53, 54C-57C, and 59C-60C (Examiner's Answer at 4.)

The appellant replies, "WRSEL, 38j, 54T-57T, 59T-60T, 53, 54C-57C and 59C-60C of McClure are not local data write driver circuits to memory cells 30." (Reply Br. at 10.) We disagree with the appellant and also disagree with the examiner.

The appellant errs by attempting to read limitations from the specification into the claims. "In the patentability context, claims are to be given their broadest reasonable interpretations. Moreover, limitations are not to be read into the claims from the specification." In re Van Geuns, 988 F.2d 1181, 1184, 26 USPQ2d 1057, 1059 (Fed. Cir. 1993) (internal citations omitted). Each of claims 22-28 specifies in pertinent part "[a] sense amplifier arrangement for an integrated circuit memory comprising ... first and second local data write driver circuits" Things that are local, "hav[e] a definite spatial form or location." Webster's Ninth New Collegiate Dictionary 700 (1990). Giving the limitations

their broadest reasonable interpretation, each of the claims recites data write driver circuits that have a definite spatial form or location.

Figure 5 of McClure shows that elements 54T-57T, 59T-60T, 53, 54C-57C and 59C-60C form specific circuitry that is located inside the reference's sense amplifier 13j. See also col. 10, l. 51 - col. 11, l. 28 (referring to Fig. 5.)
Because the elements

have a definite spatial form or location, McClure teaches the claimed "sense amplifier arrangement for an integrated circuit memory comprising ... first and second local data write driver circuits"

Nevertheless, each of claims 22-28 also specifies in pertinent part "[a] sense amplifier arrangement for an integrated circuit memory comprising: a latch" In other words, each of the claims recites a latch circuit that is part of a sense amplifier.

The examiner again errs in determining the content of the prior art. Although he refers to memory cells 30 of McClure, the memory cells 30 are not part of the reference's sense amplifiers as aforementioned regarding the novelty of claims 8, 9, 14-21, 29, 30, 32, 33, and 50. Accordingly, the examiner fails to show a teaching of the claimed "sense amplifier arrangement for an integrated circuit memory comprising: a latch" The absence of this showing negates anticipation. Therefore, we reverse the rejection of claims

22-28 under 35 U.S.C. § 102(e). Next and last, we address the novelty of claims 40-49.

Novelty of Claims 40-49

Regarding claims 40-49, the examiner makes the following assertion:

McClure shows ... at least one pair of bit lines SN-SN- of the memory; a local data write driver circuit WRSEL, 38j, 54T-57T, 59T-60T, 53, 54C-57C, and 59C-60C coupled to the latch circuit 48, the driver circuit including a plurality of transistors coupled together; the local data write driver circuit being respectively coupled to a data write control signal 38j and WRSEL so that a power supply voltage (Vcc inside 48) may be (note that "may be" is a broad term so that the Examiner can interpret it as "may be not") selectively coupled via the local data write driver circuit to an internal node of the latch circuit 48 and thus to a corresponding bit line SN-SN-, in accordance with the data write control signal 38j and WRSEL (note that the power supply voltage VCC inside 48 may not be selectively coupled to the latch circuit because of an isolation signal ISO to pass transistors 43). (Examiner's Answer at 5-6.)

The appellant replies, "circuit 48 of McClure does not have a power supply voltage selectively coupled via a local data

write driver to an internal node of a latch circuit *and thus to a corresponding bit line*" (Reply Br. at 11.) We agree with the appellant.

Each of claims 40-49 specifies in pertinent part the following limitations:

a sense amplifier latch circuit having internal nodes coupled directly or selectively to at least one pair of bit lines of the memory;

. . .

said local data write driver circuit being responsively coupled to a data write control signal so that a power supply voltage may be selectively coupled via said local data write driver circuit to an internal node of said latch circuit and thus to a corresponding bit line, in accordance with said data write control signal.

Giving the limitations their broadest reasonable interpretation, each of the claims recites driving a bit line during write operations.

The examiner fails to show a teaching of this limitation in the prior art. Although he refers to McClure's sense nodes SN and SN₋, the sense nodes are "complementary lines on the opposite side of pass transistors 43 from input/output lines 21_j and 21_{j-}" Col. 9, ll. 45-46. "[E]ach of pass transistors 43 ha[s] its gate controlled by an isolate signal ISO." Id. at ll. 40-41. "ISO will be driven to a high logic level during

write operations to turn off pass gates 43, so that data written by the write side of sense/write circuits 13 will not be sensed by sense amplifiers 48 and output onto output bus 20 during such operations." Col. 14, l. 68 - col. 15, l. 5. Because pass transistors 43 are turned off during write operations, lines SN and SN₋ are not driven during write operations. Accordingly, the examiner fails to show a teaching of the claimed "power supply voltage [that] may be selectively coupled via said local data write driver circuit to an internal node of said latch circuit and thus to a corresponding bit line, in accordance with said data write

control signal." The absence of this showing negates anticipation. Therefore, we reverse the rejection of claims 40-49 under 35 U.S.C. § 102(e).

CONCLUSION

To summarize, the examiner's rejection of claims 8, 9, 14-30, 32, 33, and 40-50 under 35 U.S.C. § 102(e) is reversed.

REVERSED

ERROL A. KRASS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
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