

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte YUKIO SUZUKI

Appeal No. 1997-2292
Application 08/483,839¹

ON BRIEF

Before HAIRSTON, JERRY SMITH, and RUGGIERO, Administrative
Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1
and 2.

The disclosed invention relates to a semiconductor

¹ Application for patent filed June 15, 1995. According to applicant, the application is a continuation of Application 08/229,155, filed April 18, 1994, which is abandoned.

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integrated circuit for producing a program control signal only when a given number of clock pulses are detected during a period when a trigger signal changes from a first state to a second state.

Claim 1 is the only independent claim on appeal, and it reads as follows:

1. A semiconductor integrated circuit comprising:

a clock number-detecting circuit for detecting a number of clocks of a serially input pulse train, said clock number-detecting circuit having an input port for receiving said serially input pulse train and an output port for providing an output signal having a given form only when the serially input pulse train has a predetermined number of clocks; and

a program control circuit for delivering a program instruction to a memory, said program control circuit having a first input port coupled to said clock number-detecting circuit output port for receiving said clock number-detecting circuit output signal, a second input port for receiving a trigger signal and an output port for supplying said program instruction, wherein said program control circuit delivers said program instruction only when the signal received at said first input port has the given form while said trigger signal changes from a first state to a second state to prevent writing error data to the memory.

The references relied on by the examiner are:

Lefebvre et al. (Lefebvre)	4,873,666	Oct. 10, 1989
Gedah et al. (Gedah)	4,873,667	Oct. 10, 1989

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Claims 1 and 2 stand rejected under the first, the second and the sixth paragraphs of 35 U.S.C. § 112.

Claims 1 and 2 stand rejected under 35 U.S.C. § 102 (a, b, e, and/or g) as being anticipated by or, in the alternative,

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under 35 U.S.C. § 103 as being unpatentable over either Lefebvre or Geadah.

Reference is made to the briefs and the answer for the respective positions of the appellant and the examiner.

OPINION

For all of the reasons expressed by the appellant in the briefs, and for the additional reasons expressed infra, we will not sustain any of the rejections.

The examiner has presented a myriad of reasons for rejecting claims 1 and 2 under the first, the second and the sixth paragraphs of 35 U.S.C. § 112. It appears that the underlying reason for all of these rejections is that the disclosure does not present the detail circuitry of the program control circuit 1 and the clock number-detecting circuit 2 (Figure 1).

At the outset, we agree with the appellant (Brief, pages 9 and 10) that the examiner's rejection under the sixth paragraph of 35 U.S.C. § 112 is not proper, and it is hereby reversed.

Turning next to the indefiniteness rejection of claims 1 and 2, we agree with the appellant (Brief, pages 8 and 9) that

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the examiner has not set forth any reason(s) why certain statements in the claims are indefinite. "Claim 1 is quite clear and straightforward in its recitation of the exact relation which exists between the inputs and output of each component circuit" (Reply Brief, page 3). Thus, the rejection of claims 1 and 2 under the second paragraph of 35 U.S.C. § 112 is reversed.

With respect to the non-enablement rejection of claims 1 and 2, the appellant explains (Brief, pages 5 and 6) that:

A circuit according to the present invention is composed of two components, each of which is relatively simple. The first component is a clock-number detecting circuit whose only function, as defined in claim 1, is to provide an output signal having a given form only when the serially input pulse train has a predetermined number of clocks. Thus, this circuit is only required to count the number of clocks in a pulse train and determine whether or not the train contains a given number of clicks, or clock pulses.

The second component of the circuit defined in claim 1 is a program control circuit having a first input port connected to receive the output signal from the clock-number detecting circuit and a second input port for receiving a trigger signal. The only function of the program control circuit is to deliver a program instruction to a memory when the signal at the first input port has the given form at a time when the trigger signal applied to the second input port changes from one state to another.

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The signal diagrams forming part of the present application provide a significant amount of information to those skilled in the art because it is common practice in the digital arts to use such diagrams to describe circuit components, and particularly simple circuit components. In fact, the waveform diagrams not only make a significant contribution to satisfaction of the enablement requirement, but also identify the range of equivalents of circuits according to the present invention. In effect, any digital circuit that will produce the signal KCOUNT in response to the input signal SK can serve as a suitable clock number-detecting circuit, and any digital circuit that will produce the signal PGCY in response to the combination of input signals KCOUNT and CS can be used as a program control circuit in an integrated circuit according to the present invention. Any one skilled in the design of digital logic circuits could devise suitable clock number-detecting and program control circuits based solely on the waveform diagrams shown in Figs. 3.

We agree wholeheartedly with the appellant's assessment of the enablement of the disclosed and claimed invention "because reduction of this invention to practice, based on the entirety of the disclosure in the application, requires virtually no experimentation" (Brief, page 7). In summary, the lack of enablement rejection of claims 1 and 2 under the first paragraph of 35 U.S.C. § 112 is reversed because Figure 3 considered alone provides "all of the information that one skilled in the art would require, as of the date [of] the

subject invention, to construct operative embodiments of the invention . . ." without undue experimentation² (Reply Brief, page 7).

Turning lastly to the prior art rejections of claims 1 and 2, we agree with the examiner (Answer, page 6) that both Lefebvre and Geadah have "'write counter' means 117 which count clock pulses from CLOCK A and then send this count information to a comparator where an 'empty' or 'full' indication is given." On the other hand, we agree with appellant (Reply Brief, pages 6 and 7) that "the Examiner has not identified any specific portions of the circuits disclosed in the applied references which provide an output signal having a given form only when the input pulse train has a pre-determined number of clocks, or which deliver a program instruction only when the output signal from the clock-numbered detecting circuit has a given form while a signal changes from a first state to a second state." In the absence of such an identification by the examiner, the 35 U.S.C. § 102

² In view of the reversal of this rejection, we will not address the merits of appellant's declaration (paper number 9).

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and 35 U.S.C. § 103 rejections of claims 1 and 2 are reversed.

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DECISION

As indicated supra, all of the rejections are reversed.
Accordingly, the decision of the examiner is reversed.

REVERSED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
)	
)	
)	BOARD OF PATENT
JERRY SMITH)	APPEALS AND
Administrative Patent Judge)	INTERFERENCES
)	
)	
JOSEPH F. RUGGIERO)	
Administrative Patent Judge)	

KWH:svt

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