

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 32

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TSUNENORI UMEKI and HIROHIKO INOUE

Appeal No. 97-1205
Application No. 08/357,551¹

ON BRIEF

Before THOMAS, BARRETT, and GROSS, Administrative Patent Judges.
GROSS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claim 5.

The disclosed invention relates to a method for a micro-computer to access code from memory. The instruction codes accessed from a high-speed memory are fetched directly to the

¹ Application for patent filed December 16, 1994.

CPU, whereas codes accessed from a low-speed memory are fetched to the instruction queue buffer and then to the CPU one cycle later. Claim 5 is illustrative of the claimed invention, and it reads as follows:

5. In a microcomputer, a method for a central processing unit (CPU) to fetch an instruction code from a memory when an instruction queue buffer does not contain the instruction code, comprising the steps of:

fetching the instruction code from a high-speed memory directly to the CPU, if the instruction code is in said high speed memory;

fetching the instruction code from a low-speed memory to the instruction queue buffer, if said instruction code is in said low-speed memory;

waiting until said instruction code is fetched from said low-speed memory into said instruction queue buffer; and

fetching the instruction code from the instruction queue buffer to the CPU, one cycle after the instruction code has been fetched from said low-speed memory to the instruction queue buffer.

The prior art reference of record relied upon by the examiner in rejecting the appealed claim is:

Matsuo et al. (Matsuo)

4,796,175

Jan. 03,

1989

Claim 5 stands rejected under 35 U.S.C. § 103 as being unpatentable over Matsuo.

Reference is made to the examiner's answer (Paper No. 25, mailed June 24, 1996) for the examiner's complete reasoning in support of the rejections, and to the appellants' briefs (Paper Nos. 22 and 24, filed March 1, 1996 and April 1, 1996, respectively) and reply brief (Paper No. 27, filed August 26, 1996) for the appellants' arguments thereagainst.

OPINION

We have carefully considered the positions of the examiner and the appellants and we will reverse the obviousness rejection of claim 5.

Claim 5 requires an instruction code fetched from a high-speed memory to go "directly to the CPU", whereas an instruction code fetched from a low-speed memory goes first into the instruction queue buffer and then to the CPU. The examiner is of the opinion (Answer page 6) that Matsuo "explicitly disclose fetching the instruction code from a high-speed memory (i.e. cache memory) directly to the CPU if the instruction code is in the high-speed memory, and fetching

the instruction code from a low-speed memory (i.e. main memory) to the instruction queue buffer if the instruction code is in the low-speed memory." The examiner refers to the abstract, and column 1, line 10-column 4, line 47, or rather the entire patent, to support his assertion. Appellants, on the other hand, argue (Brief, pages 7-9) that

instruction codes from the cache memory (high-speed memory) are placed in the instruction queue buffer before going to the CPU. We do not find the teachings of Matsuo to support the examiner's statements and, therefore, agree with appellants.

Matsuo disclose in column 2, lines 55-59, "when an amount of instruction data stored in the instruction queue 1 decreases to an amount below a constant value, ... the instruction queue 1 searches the instruction cache 4." In column 3, lines 11-16, Matsuo teach that when "the cache was hit, the instruction queue 1 queues the instruction data stored in the instruction cache 4. Therefore, there is no need to wait until the instruction is fetched from the main memory and the possibility such that the instruction queue becomes empty can be reduced." In other words, instructions

from the high-speed memory (the instruction cache 4) are fetched to the instruction queue 1, so that the queue does not become empty, and therefore are not fetched directly to the CPU, as recited in claim 5. Furthermore, as pointed out by appellants (Brief, page 7), Figure 1 of Matsuo shows the instruction cache feeding directly into the instruction queue

only. Accordingly, all data fetched from the instruction cache 4 must go to the instruction queue 1, and not directly to the CPU.

Regarding the recitation of waiting one cycle between fetching instruction codes from the slow-speed memory to the instruction queue buffer and fetching the codes from the instruction queue buffer to the CPU, the examiner admits that Matsuo does not explicitly disclose any delay (Answer, page 4). Although the examiner attempts to explain why it would have been obvious to one of ordinary skill in the art at the time of the invention, he fails to provide any evidence to support his rationale.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988); Stratoflex Inc. V. Aeroquip Corp., 713 F.2d 1530, 1535, 218 USPQ 871, 876 (Fed. Cir. 1983); In re Warner, 379 F.2d 1011, 1016, 154 USPQ 173, 177 (CCPA 1967), cert. denied, 389 U.S. 1057. In so doing, the examiner is required to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. V. Rudkin-Wiley, 837 F.2d 1044, 1052, 5 USPQ2d 1434, 1439 (Fed. Cir. 1988); Ashland Oil, Inc. V. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985); ACS Hospital Systems, Inc. V.

Montefiore Hospital, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984); In re Sernaker, 702 F.2d 989, 994, 217 USPQ 1, 5 (Fed. Cir. 1983).

In the present case, the examiner's reasons for obviousness have not come from any teaching, suggestion or implication in the prior art as a whole, nor has he alleged knowledge generally available to one having ordinary skill in the art as to why it would have been obvious to one of ordinary skill in the art to wait one cycle after fetching the instruction code to the instruction queue before fetching the code to the CPU. Accordingly, the examiner has failed to establish a prima facie

case of obviousness. Based upon the foregoing, the rejection of claim 5 under 35 U.S.C. § 103 cannot be sustained.

DECISION

To summarize, the decision of the examiner to reject claim 5 under 35 U.S.C. § 103 is reversed.

REVERSED

JAMES D. THOMAS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
LEE E. BARRETT)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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ANITA PELLMAN GROSS)	
Administrative Patent Judge)	

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