

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today  
(1) was not written for publication in a law journal and  
(2) is not binding precedent of the Board.

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte TAWADA SHIGEYOSHI

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Appeal No. 1997-1185  
Application 08/497,845<sup>1</sup>

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Heard: December 07, 1999

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Before FLEMING, RUGGIERO and HECKER, Administrative Patent Judges.

HECKER, Administrative Patent Judge.

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<sup>1</sup> Application for patent filed July 03, 1996. According to appellant, this application is a continuation of 07/996,621 filed December 24, 1992.

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DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 19, all claims pending in this application. The invention relates to a method for designing clock wiring in, for example, a Large Scale Integrated Circuit (LSI). The invention is based on the recognition that a shorter clock period can be established if one ignores the conventional rule of providing a zero clock skew between clock nets. In particular, looking at Figure 4, if a 2 nanosecond delay gate 217 is inserted between clock driver 202 and flip-flop 205, causing a 2 nanosecond skew between the clock nets to flip-flops 204-206, a clock period of 8 nanoseconds can be employed instead of a clock period of 10 nanoseconds which would have been mandated by the delay of the worst case path. To shorten the clock cycle, the invention evaluates delay time margins for a plurality of paths (in this case, a zero delay time margin for path 215 and a 4 nanosecond delay time margin for path 216), detects a worst case path (path 215), calculates a clock skew adjusting time by determining a difference between the delay time margin of a secondary worst case path (4 nanoseconds of 216) and the

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worst delay time margin (zero nanoseconds of path 215),  
determines an optimum delay time to be added to a clock net  
leading to a clock

input terminal at a terminal side of the worst case path  
(e.g., 4  
nanoseconds/2 = 2 nanoseconds), and inserts a delay (217) into  
the clock net.

Representative independent claim 1 is reproduced as  
follows:

1. A clock wiring designing apparatus for designing  
clock wiring of an LSI, PWB or the like, said clock wiring  
designing apparatus comprising:

delay analyzing means for evaluating delay time  
margins for a plurality of paths;

means for detecting a worst case path having a  
worst delay time margin among the delay time margins;

means for calculating a clock skew adjusting  
time by determining a difference between a delay time margin;

additional delay time calculating means for  
determining an optimum delay time to be added to a clock net  
leading to a clock input terminal at a terminal side of the  
worst case path within a range of the clock skew adjusting  
time; and

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means for inserting a delay gate in said clock net so that the delay time determined by the additional delay time calculating means is added to the clock net as an additional clock skew, whereby a total time margin is used between said worst case path and said secondary worst case path.

The Examiner relies on the following references:

Hooper                    5,168,455                    Dec. 1, 1992 (filed Mar. 28, 1991)

Hitchcock, Sr. et al., "Timing Analysis of Computer Hardware", IBM J. Res. Develop., Vol. 26, No. 1, pp. 100-105, Jan. 1982

Claims 1 through 19 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hooper in view of Hitchcock.

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the brief and answer for the respective details thereof.

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OPINION

After a careful review of the evidence before us, we will not sustain the rejection of claims 1 through 19 under 35 U.S.C. § 103.

The Examiner has failed to set forth a *prima facie* case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the reasonable teachings or suggestions found in the prior art, or by a reasonable inference to the artisan contained in such teachings or suggestions.

*In re Sernaker*, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." *Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.*, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995) (*citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed.

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Cir. 1983), **cert. denied**, 469 U.S. 851 (1984)).

The Examiner states that Hooper discloses a data processing system for analyzing timing in the synthesis of logic circuits and uses a multipath delay analysis based on worst delay path. The Examiner reasons that Hooper is applicable to clock wiring design and analysis because both Hooper and Appellant's invention are directed to signal propagation in a wiring net or media. The Examiner notes that Hooper discloses a latch circuit to meet timing performance but does not explicitly disclose inserting a delay gate as claimed. The Examiner contends that such a feature is well known as shown by Hitchcock which uses timing analysis and timing adjustment to meet circuit performance. This would motivate those skilled in the art to use gate delay as a means to improve timing performance because the

gate delay would provide a delay time to meet clock synchronization. (Answer-pages 3 and 4.)

Appellant agrees that timing considerations are a

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critical factor in circuit design. But, Appellant argues, Hooper and Hitchcock are directed to **circuit component selection** based on a **timing budget** and a **fixed clock rate**. Both fail to teach **adjusting the clock rate**. (Brief-pages 5 and 6.) At page 7 of the brief Appellant states:

Like Hooper, this [Hitchcock] is all part of the layout and selection of circuit components, and is not related to the establishment of a clock net for selected components.

The Examiner cites several instances where the references determine and adjust clock delay, and concludes that clock rate adjustment is clearly disclosed (answer-page 6). We take issue with this reasoning, adjusting clock delay is not a clock rate adjustment. Note Appellant's prior art Figure 2 with a clock rate of 10 nanoseconds versus Figure 5 showing an improved clock rate of 8 nanoseconds.

Appellant's independent claim recites "determining a difference between a delay time margin of a **secondary worst case** path and the **worst delay** time margin;", (emphasis added) claim 1, lines 9 and 10. Similar language can be found in claims 2 and 3, at lines 9 and 10; claim 6, lines 15 and 16; and claim 7,

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lines 7 and 8 (all independent claims of this application). This difference is used to calculate the additional time delay added to the **clock net**. Hooper and Hitchcock adjust time delays by changing circuit components, without changes to the clock net. Note Hitchcock, where it states:

From Fig.2, one can observe a funneling of negative slack values through block BA. If BA could be **replaced by a circuit having a smaller delay**, all the negative slacks could be eliminated without changing functional design at all. (Page 102, right column, second full paragraph.) (Emphasis added.)

Similarly, Hooper states in the abstract:

The timing debt can be used as a criterion to determine when the implementation of **circuit component should be changed**. (Emphasis added.)

Although the Examiner has noted instances of using delay in the clock net (e.g., Hooper, column 5, lines 31-47), the claimed calculation recited supra, using the worst delay time margin and the secondary worst delay time margin, is not disclosed or suggested by the references.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification."

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***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." ***Para-Ordnance Mfg. v. SGS Importers Int'l***, 73 F.3d at 1087, 37 USPQ2d at 1239, ***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13.

As pointed out above, the applied references teach circuit time analysis and modification by changing circuit components. Appellant claims clock net analysis and changes to the clock net. Thus, we will not sustain the Examiner's rejection of independent claim 1, 2, 3, 6 and 8, and likewise, we will not sustain the rejection of the remaining dependent claims which contain the same limitations.

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We have not sustained the rejection of claims 1 through 19 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

Michael R. Fleming )  
Administrative Patent Judge )  
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) BOARD OF  
)  
Joseph F. Ruggiero ) PATENT  
Administrative Patent Judge )  
) APPEALS AND  
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INTERFERENCES  
Stuart N. Hecker )  
Administrative Patent Judge )

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