

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today  
(1) was not written for publication in a law journal and  
(2) is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte MICHIO NAKAJIMA

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Appeal No. 1997-1038  
Application 08/077,926<sup>1</sup>

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HEARD: NOVEMBER 18, 1999

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Before THOMAS, KRASS, and DIXON, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellant has appealed to the Board from the examiner's final rejection of claims 1, 6 through 21 and 23 through 26.

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<sup>1</sup> Application for patent filed June 18, 1993.

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Representative claim 1 is reproduced below:

1. A semiconductor device comprising

(a) a semiconductor circuit which is an object of a test,

(b) an input terminal means receiving an input signal to the semiconductor circuit during an ordinary operation,

(c) an output terminal receiving an output signal from the semiconductor circuit during the ordinary operation,

(d) a power terminal applying a specified potential to the semiconductor circuit during the ordinary operation, and

(e) a mode switching circuit interposed between the input terminal means and the semiconductor circuit for switching its operation from the test to the ordinary operation; wherein

the mode switching circuit (e-1) applies the input signal received on the input terminal to the semiconductor circuit during the ordinary operation and

(e-2) applies at least one specified fixed value to the semiconductor circuit during the test and, wherein the mode switching circuit receives a test signal which is activated during the test and deactivated during the ordinary operation, wherein the input terminal includes first and second input terminals;

and wherein the at least one specified fixed value includes first and second fixed values,

the mode switching circuit includes a first gate for outputting the first fixed value regardless of a value of a signal applied to the first input terminal during the test and a second gate for outputting the second fixed value regardless of a value of a signal applied to the second input terminal during the test and

wherein the test signal takes the first fixed value when activated or otherwise take the second fixed value when deactivated

wherein the first and second fixed values corresponds to logical values "1" and "0", respectively, and wherein the first gate includes a first input end connected to the first input terminal, a second input end receiving the test signal, and an output end outputting a logical product of a logic value applied to the first input end thereof and an inverted logic value of the test signal to the semiconductor circuit, and the second gate includes a first input end connected to the second input terminal, a second input end receiving the test signal, and an output end outputting a logical sum of logic values of the first and second input ends to the semiconductor circuit.

There are no references relied on by the examiner.

Claims 1, 6 through 19 and 23 stand rejected under the written description portion of the first paragraph of 35 U.S.C. § 112. Claims 20, 21 and 23 through 26 stand rejected under the second paragraph of 35 U.S.C. § 112 as being indefinite.

Rather than repeat the positions of the appellant and the examiner, reference is made to the briefs and the answer for the respective details thereof.

#### OPINION

We reverse both rejections.

As to the rejection under the first paragraph of 35 U.S.C. § 112, our review of the examiner's position, appellant's arguments, as well as the specification, drawings and claims presently on appeal all lead us to conclude that the subject matter questioned by the examiner as to claims 1, 6 through 19 and 23 was adequately described in the specification as filed to indicate that the appellant had possession of the presently claimed invention as of the filing date of the application.

At the outset, we note that the examiner's summary of the invention comment on page 2 of the answer takes the view that the first and second gates are respective gates 16b and 16a. However, the specification as filed has consistently indicated that the claimed first gate comprises gate 16a and the second gate comprises gate 16b, respectively, just the opposite of the examiner's view. Note, for example, the summary of the invention at page 4, lines 10 through 18 of the specification, as well as the showing at least in the first embodiment of Figure 1 and the description at page 16, lines 5 through 13 of the specification as filed, as argued by appellant at page 6 of the brief. Therefore, we are in agreement with the appellant's conclusion at the end of that page of the brief that there is no inconsistency of the language recited in claim 1 within the claim itself, nor is there any inconsistency with the claim language and the specification and drawings as filed. Functionally speaking, the noted first gate of the claim, as well as the first gate of the specification, provides an output of a logical product, whereas the second gate similarly provides a logical sum.

We reach a similar conclusion with respect to the separate concerns raised by the examiner as to dependent claim 23, which depends from claim 21, which in turns depends from independent claim 20. Since claim 20 recites a semiconductor wafer, this is an indirect reference to the initial disclosure of the embodiment shown in Figure 8 depicting the recited dicing line 30 and the signal generating means 17, 18 depicted in Figure 10 following the general depiction in Figure 8. The Figures 9 and 10 details indicate clearly

the showing of a first fuse 27 interconnecting the metal wiring 25a by means of a wiring 29a. As to the particulars of the second fuse interposed between the signal generating means 17, 18 and the semi-conductor circuit (generally the ICs 102a of Figure 8), there appears to be no clear depiction of the drawings of any claimed second fuse of claim 23. However, appellant is correct in recognizing that the specification at page 25, lines 3 through 6 teaches by written description alone that there is at least one other or a second fuse connected in the manner claimed. This may be taken as the fuse taught at the output terminal 35 of the waveform generator 18 and also "in the course of the wiring 29c," which appears to indicate that the wiring 29c itself would be considered a second fuse because its width is identical to the width comprising a normally depicted fuse 27, that is, a relatively narrow width compared to the other wiring layers and contact hole showings.

Therefore, the disputed recitations noted by the examiner as to independent claim 1 and dependent claim 23 have been adequately shown by appellant and noted here by us to have been possessed by appellant in the specification as filed. As such, the rejection of the noted claims under the first paragraph of 35 U.S.C. § 112 is reversed.

Turning lastly to the rejection of certain claims under the second paragraph of 35 U.S.C. § 112, the examiner's view is, that clause (b) in claim 20 relating to a second wiring is not clear as to how a single second wiring is commonly connected to the first wiring of the plurality of semiconductor devices. Without belaboring the issue, a showing in the

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embodiments with respect to Figures 8 through 10 and the discussion of Figures 8 and 9 beginning at the bottom of specification page 22 as filed through the top of page 23 at least indicate that metal wiring 25a is commonly connected via a contact hole 26 to a plurality of integrated circuits. Specification page 23, lines 6 through 8 indicate that the connection between the metal wiring 25a and the wiring 29a "is in the contact hole 26" while at the same time a connection of the opposite or other end terminal of the fuse 27 "is in the contact hole 28" depicted in Figure 9 (emphasis added). A study of the examiner's expanded views of this issue at page 7 of the answer leads us to conclude that the examiner appears to have answered his own question. In any event, we fail to see any ambiguity or indefiniteness in the recitation noted by the examiner with respect to clause (b) of independent claim 20 on appeal.



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