

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MICHAEL SCHLANSKER, RAMAKRISHNA RAU, and VINOD KATHAIL

Appeal No. 1997-0923
Application No. 08/400,414¹

ON BRIEF

Before KRASS, BARRETT, and GROSS, Administrative Patent Judges.
GROSS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 21 through 47, which are all of the claims pending in this application. In the Examiner's Answer (page 8), the examiner withdraws the rejection of claims 26 and 34.

¹ Application for patent filed March 3, 1995. According to appellants, this application is a continuation of Serial No. 08/166,582, filed December 13, 1993, now abandoned.

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Although the examiner does not explicitly withdraw the rejection of claim 45, since claim 45 recites the same limitations as in claim 26 but in a device format, we assume that the rejection of claim 45 is withdrawn as well. Accordingly, claims 21 through 25, 27 through 33, 35 through 44, 46, and 47 remain before us on appeal.

The appellants' invention relates to a method for evaluating Boolean expressions in a computer system. More specifically, the method involves performing a comparison to obtain a condition value, performing a Boolean reduction function on the condition value to produce a result value, and conditionally writing the result value to a target register. Claim 21 is illustrative of the claimed invention, and it reads as follows:

21. A method of evaluating Boolean expressions and predicates in a computer system having a processor with an instruction unit for decoding instructions of an instruction set, a functional unit for executing operations specified in the decoded instructions, and a set of registers, the method comprising the steps of:

decoding instructions of a program in the instruction unit, the program's instructions being selected from the instruction set;

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executing operations specified by the decoded instructions in the functional unit, the executing of a corresponding reduction operation specified by one of the decoded instructions in any one of the at least one functional unit comprising the steps of:

retrieving at least one instruction-specified input value for the reduction operation;

producing a Boolean result value having a first instruction-specified state;

performing an instruction-specified condition function of one or more of the input values of the operation to produce a Boolean condition value, wherein the Boolean condition value is false for at least one combination of the input values; and conditionally writing the result value in an instruction-specified location in the set of registers if the Boolean condition value is a second instruction-specified state.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Connors	4,212,076	Jul. 08, 1980
Faudemay et al. (Faudemay)	5,239,663	Aug. 24, 1993

Claims 21 through 25, 27 through 33, 35, 36, 38, 41 through 44, 46 and 47 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Connors.

Claims 37, 39, and 40 stand rejected under 35 U.S.C. § 103 as being unpatentable over Faudemay in view of Connors.

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Reference is made to the Final Rejection (Paper No. 15, mailed December 29, 1995) and the Examiner's Answer (Paper No. 19, mailed July 24, 1996) for the examiner's complete reasoning in support of the rejections, and to the appellants' Brief (Paper No. 17, filed May 8, 1996) for the appellants' arguments thereagainst.

PROBLEMS WITH THE CLAIMS

In claim 21, the limitation of "producing a Boolean result value having a first instruction-specified state" seems to imply that the result value is not dependent on the condition value. However, as discussed with respect to appellants' table 3, the result value is determined from the condition value.

Accordingly, it is not apparent how the step of "producing a Boolean result value having a first instruction-specified state" can occur before the step of "performing an instruction-specified condition function," since it depends on the result of the condition function. A more appropriate ordering of the steps would seem to be (1) "retrieving at least one instruction-specified input value for the reduction operation," (2) "performing an instruction-specified condition

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function of one or more of the input values," (3) "producing a Boolean result value," and (4) "conditionally writing the result value in an instruction-specified location."

Additionally, it is unclear to say that the result value is conditionally written "if the Boolean condition value is a second instruction-specified state" (last subparagraph of claim 21) when no first instruction-specified state has been defined for the condition value; the first instruction-specified state is for the result value. Furthermore, it seems misdescriptive to say that the condition value "is a second instruction-specified state"; the condition value is obtained by performing an instruction-specified function on input data. According to the discussion of appellants' table 3, the conditional writing of the result value depends on the state of the result value, not on the instruction nor the condition value.

OPINION

We have carefully considered the claims, the applied prior art references, and the respective positions articulated by the appellants and the examiner. As a consequence of our review, we will reverse both the anticipation rejection of

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claims 21 through 25, 27 through 33, 35, 36, 38, 41 through 44, 46 and 47 and also the obviousness rejection of claims 37, 39, and 40.

The examiner asserts that Connors anticipates claim 21.

The examiner states (Final Rejection, page 5):

Col. 31, line 27 et seq. describes the evaluation of a Boolean expression. Col. 43 line 36 et seq. describes the evaluation of an expression containing logical expressions and comparisons ("N2 is positive" is equivalent to "N2>0"). Connors discussed "conditional" execution of an operation (including subsequent Boolean operations) throughout his specification; for example col. 13, line 63 et seq. discusses execution of an instruction based on whether a bit=0 or 1.

In the Answer (page 5), the examiner contends that claim 21 is no more than the evaluation of "IF (A op C)=B2; THEN R=B1."

The examiner continues, "Since any computer or microprocessor is comprised of various registers and functional units internally to its CPU or ALU, and contains instruction registers, decoders, etc.; a wide variety of machines may evaluate the above expression" (underlining added for emphasis). In the Answer (page 6), the examiner further refers to Connors' statement that

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it is possible to program instructions to be conditional or unconditional. However, the examiner fails to specifically point out how the particular above-referenced portions of Connors are interrelated to meet the claimed limitations. The examiner's position seems to be that since key words such as "Boolean" and "condition" appear somewhere in Connors, the claims are anticipated.

As pointed out by appellants (Brief, page 17), "Connors' execution of Boolean operation instructions also lacks conditionally writing as claimed." When Connors executes a Boolean operation, the result value is held in a flip-flop 425 within the computers CPU (column 32, lines 15-19). Connors does not conditionally write to a register depending on either the condition value or the result value. Comments about conditions in Connors refer to whether the execution of a function is to be conditional or unconditional. Accordingly, we find that Connors does not anticipate claim 21 or its dependents, claims 22 through 25, 27 through 33, 35, and 36. In addition, since claim 38 is substantially the same as claim 21 but in device format, claim 38 and its dependents, claims 41 through 44, 46 and 47 are not anticipated by Connors.

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Claims 37, 39, and 40 each recite that multiple functional units write to the same register simultaneously. The examiner relies on Faudemay and Conners as evidence of obviousness. The examiner states (Final Rejection, page 7) that "[a]lthough Faudemay does not discuss the use of registers . . . for storing results; Conners discloses the use of a small memory to store results, operands, etc." The examiner concludes that it would have been obvious "to provide registers or some means of storing results for use in future operations." The examiner, however, fails to address the limitation of writing by multiple functional units to the same register simultaneously. In the Answer, page 9, the examiner asserts that "[t]he register to which claims 37 and 39 and 40 refer appears to be the input latches to an AND functional unit or AND gate. An AND gate produces a "TRUE" result if all inputs are TRUE." The relevance of this statement to the limitation of plural units writing simultaneously to a register eludes us. As Faudemay does not even discuss registers, as admitted by the examiner, Faudemay clearly cannot disclose a register to which multiple units write concurrently. Further, the

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examiner has pointed to nothing nor can we find any disclosure in Connors that would overcome this deficiency.

In addition, claims 37, 39, and 40 depend from claims 21 and 38, respectively, and thus include the recitation of conditionally writing to the register. As discussed above, Connors does not disclose conditionally writing to the register.

Since Faudemay does not discuss registers at all, Faudemay cannot cure the defect of Connors. Accordingly, we cannot sustain the obviousness rejection of claims 37, 39, and 40.

CONCLUSION

The decision of the examiner rejecting claims 21 through 25, 27 through 33, 35, 36, 38, 41 through 44, 46 and 47 under 35 U.S.C. § 102(b) is reversed. The decision of the examiner

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rejecting claims 37, 39, and 40 under 35 U.S.C. § 103 is
reversed.

REVERSED

ERROL A. KRASS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
LEE E. BARRETT)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
)	
)	
)	
ANITA PELLMAN GROSS)	
Administrative Patent Judge)	

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