

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 35

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JAMES LIOU and THEODORE W. HOUSTON

Appeal No. 97-0557
Application 08/371,040¹

ON BRIEF

Before HAIRSTON, BARRETT and LALL, Administrative Patent Judges.

LALL, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134

¹ Application for patent filed January 10, 1995. According to Appellants, the application is a continuation of application 08/186,215, filed January 24, 1994, now abandoned, which is a continuation of Application 08/015,874, filed February 3, 1993, now abandoned, which is a continuation of application 07/825,743, filed January 23, 1992, now abandoned, which is a continuation of Application 07/358,298, filed May 26, 1989, now abandoned.

Appeal No. 97-0557
Application 08/371,040

from the Examiner's final rejection² of claims 13 through 17, all the pending claims in the case.

The disclosed invention pertains to an architecture for distributing input signals from a bondpad area to an interior portion of an integrated circuit device, such as a plurality of memory blocks. Instead of placing input buffers at the periphery of the integrated circuit device, the claimed invention distributes the unbuffered input signal lines to the input buffers located in the interior portion of the integrated circuit adjacent the circuit blocks that use the input signals.

Representative claim 13 is reproduced as follows:

13. An input architecture for supplying a plurality of signals to a plurality of circuit blocks located in an interior portion of an integrated circuit device, comprising:

a bondpad area;

a plurality of input buffers each located adjacent to and connected to one of said plurality of circuit blocks;

a plurality of unbuffered signal lines, each of said plurality of unbuffered signal lines connected between said bondpad area and all of said plurality of input buffers.

² An amendment after the final rejection was filed on April 23, 1996 [paper no. 30] and entered in the record.

Appeal No. 97-0557
Application 08/371,040

The Examiner relies on the following reference:

Takemae et al. al. (Takemae) 21, 1987	4,660,174	Apr.
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Claims 13 through 17 stand rejected under 35 U.S.C. § 102 as being anticipated by Takemae.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the brief and the answer for the respective details thereof.

OPINION

We have considered the rejections advanced by the Examiner and the supporting arguments. We have, likewise, reviewed the Appellants' arguments set forth in the brief.

It is our view that claims 13 through 17 are not anticipated by Takemae. Accordingly, we reverse.

In our analysis, we are guided by the precedence of our reviewing court that anticipation under 35 U.S.C. § 102 is established only when a single prior art reference discloses, either expressly or under the principles of inherency, each and every element of a claimed invention. See RCA Corp. V. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444, 221

Appeal No. 97-0557
Application 08/371,040

USPQ 385, 388 (Fed. Cir.), cert dismissed, 468 U.S. 1228
(1984).

Rejection of Claims 13 through 17 under 35 U.S.C. § 102

The Examiner has rejected these claims as being anticipated by Takemae. We take claim 13 as representative. We have considered Appellants' arguments [brief, pages 3 and 4] and Examiner's position [answer, pages 3] in regard to claim 13. We find that Takemae does not anticipate claim 13. For example, Takemae does not show the limitation: "a plurality of input buffers each located adjacent to and connected to one of said plurality of circuit blocks;" (claim 13, lines 4 to 5). The Examiner contends that "[T]he claimed 'plurality of input buffers' correspond to the row and column decoders 105-107 in array 1-1 and 1-2." [Answer, page 3]. We agree with the Examiner that each of elements 105-107 serve as decoders for each word line and each bit line [column 4, lines 16 to 28], however the Examiner has not shown specifically a plurality of input buffers each located adjacent to and connected to one of said plurality of circuit blocks. The Examiner has not presented any argument where such buffers are

Appeal No. 97-0557
Application 08/371,040

disclosed, explicitly or implicitly or inherently, in Takemae. Appellants already admit in their disclosure [for example, figure 1a] that there is a decoder DC in a line to each circuit block. Takemae is primarily concerned with reducing the total line width of the signal and power supply lines linking the peripheral circuit areas and the pads and bypassing the divided regular circuit areas, thereby increasing the regular circuit area and hence increasing the capacity of the memory [column 2, lines 18 to 29]. Takemae offers little in the way of circuit connections in the manner shown, for example, in figures 1 and 2 of the Appellants' disclosure. We, therefore, conclude that the anticipation rejection of claim 13 over Takemae is not sustainable. As for the other independent claim 17, it also contains a corresponding limitation, namely, "a plurality of input buffers, each ... located proximate to and connected to one of said decode circuits;" (claim 17, lines 6 to 7). Therefore, the anticipation rejection of claim 17 is also not sustained. Since claims 14 through 16 depend on claim 13 and contain at least the claimed limitation discussed above regarding claim 13, their anticipation rejection over Takemae is also not

Appeal No. 97-0557
Application 08/371,040

sustained.

In conclusion, we reverse the decision of the Examiner rejecting claims 13 through 17 as being anticipated by Takemae under 35 U.S.C. § 102.

REVERSED

	KENNETH W. HAIRSTON)	
	Administrative Patent Judge)	
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	LEE E. BARRETT)	BOARD OF
PATENT	Administrative Patent Judge)	APPEALS AND
)	INTERFERENCES
)	
)	
	PARSHOTAM S. LALL)	
	Administrative Patent Judge)	

Jacqueline J. Garner
Texas Instruments Incorporated
Patent Department M S 219
P. O. Box 655474
Dallas, TX 75262

PSL/ki