

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHRISTIAN JOLY, ZARIR SARKARI, RAVICHANDRAN RAMACHANDRAN,
SARIKA AGRAWAL and SANJAY ADKAR

Appeal No. 1997-0553
Application No. 08/409,191

ON BRIEF

Before FLEMING, RUGGIERO, and DIXON, **Administrative Patent Judges**.
DIXON, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1-28, which are all of the claims pending in this application.

We AFFIRM.

BACKGROUND

The appellants' invention relates to a synthesis shell generation and use in ASIC design. An understanding of the invention can be derived from a reading of exemplary claim 1, which is reproduced below.

1. A method for synthesizing a gate level description of an integrated circuit module including a plurality of circuit blocks from a behavioral description of the module, comprising:

synthesizing a first block in the plurality of blocks by processing the behavioral description of the first block to produce a gate level description of the first block;

generating a synthesis shell comprising a gate level description of a circuit having fewer gates than the gate level description of the first block by reducing the number of gates in the gate level description of the first circuit block, the synthesis shell having the same input load and fanout as the first block, output delay relative to clock as the first block, output drive of the first block, setup/hold constraints on input signals relative to clock as the first block, and delay from input to output for pass through signals as the first block; and

synthesizing at least one other block in the plurality of blocks by processing the behavioral description of the at least one other block with reference to the synthesis shell to produce a gate level description of the at least one other block.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Donath et al. (Donath)	4,263,651	Apr. 21, 1981
Drumm et al. (Drumm)	5,029,102	Jul. 02, 1991
Dangelo et al. (Dangelo)	5,222,030	Jun. 22, 1993

Claims 1-28 stand rejected under 35 U.S.C. § 103 as being unpatentable over Drumm in view of Donath and Dangelo.

Rather than reiterate the conflicting viewpoints advanced by the examiner and the appellants regarding the above-noted rejections, we make reference to the examiner's answer (Paper No. 12, mailed Jul. 16, 1996) for the examiner's reasoning in support of the

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rejections, and to the appellants' brief (Paper No. 11, filed Apr. 26, 1996) for the appellants' arguments thereagainst.

OPINION

In reaching our decision in this appeal, we have given careful consideration to the appellants' specification and claims, to the applied prior art references, and to the respective positions articulated by the appellants and the examiner. As a consequence of our review, we make the determinations which follow.

At the outset we note that our determination on this appeal is based upon the evidence of record on the issues before us at the time of the decision.

As stated by our reviewing court in *In re Baxter Travenol Labs.*, 952 F.2d 388, 391, 21 USPQ2d 1281, 1285 (Fed. Cir. 1991), "it is not the function of this court to examine the claims in greater detail than argued by an appellant." 37 C.F.R. § 1.192(a) states: "[t]he brief . . . must set forth the authorities and arguments on which appellant will rely to maintain the appeal. Any arguments or authorities not included in the brief will be refused consideration by the Board of Patent Appeals and Interferences." Similarly, we limit our review to the arguments raised by the appellants and the examiner.

From our review of the examiner's rejection, we find that the examiner has set forth a *prima facie* case of obviousness including a motivation for the combination of the prior art teachings. "To reject claims in an application under section 103, an examiner must

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show an unrebutted *prima facie* case of obviousness. **See In re Deuel**, 51 F.3d 1552, 1557, 34 USPQ2d 1210, 1214 (Fed. Cir. 1995). In the absence of a proper *prima facie* case of obviousness, an applicant who complies with the other statutory requirements is entitled to a patent. **See In re Oetiker**, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). On appeal to the Board, an applicant can overcome a rejection by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.” **In re Rouffet**, 149 F.3d 1350, 1355, 47 USPQ2d 1453, 1455 (Fed. Cir. 1998). Here, we find that appellants have not overcome the convincing *prima facie* case of obviousness by showing insufficient evidence of obviousness or by rebutting the *prima facie* case with secondary evidence. Therefore, we will sustain the rejection of claim 1.

As evidence of obviousness, the examiner relies upon the teachings and suggestions of Drumm, Donath and Dangelo. Essentially, the examiner relies upon the combination of Drumm and Dangelo since Donath does not teach the reduction of circuits, but only the need and use of timing information in analysis of a circuit. The examiner relies upon Dangelo to teach and suggest the various well-known relation-

ships or concerns which skilled artisans would have encountered being confronted with problems involving the synthesis of gate level circuits from a behavioral description.

Specifically, timing and loads are discussed in Dangelo. (See Dangelo at column 3.)

Appellants argue that Drumm attempts to improve the global optimization process by reducing the gate count that goes into the conventional final optimization. Appellants contrast the method of the present invention which improves the global optimization process by performing the global optimization on a circuit description in which the gate level description of at least one of the logic blocks is replaced by a synthesis shell that acts as a proxy for the gate level description of the logic block during global optimization. The shell is generated by reducing the high level description of a functional block to a gate level description and then replacing the gate

level description with a shell that preserves the essential timing and load information while eliminating one or more gates. (See brief at pages 4-5.) We disagree with appellants.

Appellants characterize the disclosed invention rather than the invention as recited in claim 1. The language of claim 1 is silent as to the use of a proxy. Further, we find that the method does not recite limitations that the logical or computational function is not necessarily being retained in the gate reduction. (See brief at page 5.)

Appellants argue that the invention can reduce the number of gates much smaller than Drumm can because the logic function does not have to satisfy the same logic

function of the original circuit block. **Id.** We do not find this argument persuasive because we find no basis in the claim language to support this argument.

Appellants argue that the invention maintains confidentiality of proprietary information, but appellants do not cite any specific language in claim 1 to support this argument. (See brief at page 6.) Alternatively, we find no support in claim 1 for this argument.

Appellants argue that the present invention improves the global optimization process rather than merely the gate level synthesis optimization. **Id.** Again, it is the language of the claim which we must address, and appellants have not cited any language in claim 1 to support this argument. Therefore, this argument is not persuasive.

Appellants argue that none of the cited references use a proxy for a functional block in which only the timing and load features of the functional block need to be maintained. **Id.** (Emphasis added.) We disagree with appellants since once again we find no support for this argument in claim 1. Therefore, since appellants have not rebutted the *prima facie* case of obviousness, we will sustain the rejection of claim 1. Being that appellants have grouped all claims as standing or falling as a single group, it follows that we will similarly sustain the rejection of claim 2-28.

CONCLUSION

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To summarize, the decision of the examiner to reject claims 1-28 under 35 U.S.C. § 103 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

MICHAEL R. FLEMING)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
JOSEPH F. RUGGIERO)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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JOSEPH L. DIXON)	
Administrative Patent Judge)	

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