

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 27

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MARK A. TAYLOR, DAVID J. GARCIA,
AND PAUL A. DUFFY

Appeal No. 96-4106
Application 08/271,238¹

ON BRIEF

Before HAIRSTON, KRASS, and BARRETT, Administrative Patent
Judges.

HAIRSTON, Administrative Patent Judge.

¹ Application for patent filed July 6, 1994. According to appellants, the application is a continuation of Application 07/709,919 filed May 31, 1991.

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DECISION ON APPEAL

This is an appeal from the final rejection of claims 4, 5, 11, 12, 26 through 28, 31 through 33 and 35 through 37. In the final rejection, claims 1 through 3, 19 through 25 and 34 were indicated as being allowable, and claims 13, 29 and 30 were listed as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In an Amendment After Final (paper number 18), claims 38 through 40 were added to the application. In an Advisory Action (paper number 20), claims 38 through 40 were added to the list of allowable claims. As a result of the withdrawal of the rejection of claims 4, 5, 11, 12 and 37 (Answer, page 3), and the allowance of these claims (Answer, page 1), claims 26 through 28, 31 through 33, 35 and 36 are the only claims that remain before us on appeal.

The disclosed invention relates to a method and apparatus that checks the proper operation of a processor unit by operating a copy of the processor unit, and by comparing the output signals from the two processor units. The operation of

the copy processor unit lags the operation of the checked processor unit by at least one clock period.

Claims 26 and 35 are illustrative of the claimed invention, and they read as follows:

26. A self-checking processor system, comprising:

first and second processor units each operating in response to instructions to produce address and data signals;

memory means for supplying the instructions to the first processor unit in response to address signals from the first processor unit;

first bus means coupling the memory means to the first processor unit for communicating address and data signals therebetween;

first circuit means, including second bus means, coupling the first bus means to the second processor unit for communicating to the second processor unit data signals from the first bus means in a manner emulating the memory means to the second processor unit; and

second circuit means coupled to first circuit means to receive and compare address and data signals produced by the first processor unit to address and data signals produced by the second processor unit to assert an error signal when a miscompare is detected.

35. A method of operating first and second substantially identical digital circuits to use the first digital circuit as a check for proper operation of the second digital circuit, the second digital circuit operating in response to a periodic clock signal to receive data and to supply therefrom second data in execution cycles measured by the periodic clock signal, the method comprising the steps of:

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providing the data to the first digital circuit at least one clock period after the data is supplied the second digital circuit, whereby the first digital circuit operates to produce first data from the data;

holding the second data from the second digital circuit;
and

then, comparing at least selected portions of the first and second data to issue an error signal if the comparing is not correct.

The references relied on by the examiner are:

Zieve et al. (Zieve) 1974	3,810,119	May 7,
McDonald et al. (McDonald) 1982	4,358,823	Nov. 9,

Claims 26 through 28 and 31 through 33 stand rejected under 35 U.S.C. § 103 as being unpatentable over McDonald.

Claims 35 and 36 stand rejected under 35 U.S.C. § 103 as being unpatentable over McDonald in view of Zieve.

Reference is made to the brief and the answer for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will sustain the obviousness rejection of claims 26 through 28, and reverse the obviousness rejection of claims 31 through 33, 35 and 36.

McDonald discloses a double redundant processor (Figure 1) that includes first and second master processors 50 and 64. When the first master processor is in an active state for processing signals, the second master processor is in a standby state. Each of the master processors includes first and second subprocessors 4 and 5 for simultaneously processing data, control and address signals, and a comparator 6 for comparing the output signals from the two subprocessors 4 and 5 (column 3, lines 7 through 22).

Appellants argue (Brief, page 8) that:

Claim 26, specifies a "first circuit means, including second bus means, coupling the first bus means to the second processor unit for communicating to the second processor unit data signals from the first bus means in a manner emulating the memory means to the second processor unit." (Claim 26, lines 11-15). Applicants are unable to find anything in McDonald et al. suggesting that data is supplied to one of the CPUs 4, 5 (Fig. 1) or the subprocessors 26, 29 (Fig. 4) indirectly, i.e., "in a manner emulating" a memory. To the contrary, Fig. 1 shows the CPUs 4, 5 connected in parallel to the memory 24 so that both CPUs 4, 5 receive the same data at the same time. Subprocessors 26, 29 are similarly connected [sic, connected] and, this direct connection of the CPUs 4, 5 used by McDonald et al. is required, in light of the fact the CPUs 4, 5 are operated in "lock step." (See McDonald et al., column 1, lines 63-65.) In addition, claim 26 includes "second circuit means coupled to the first circuit means to receive and compare address and

data signals produced by the first processor unit to address and data signals produced by the second processor unit to assert an error signal when a miscompare is detected." (Claim 26, lines 16-20). Again, the structure of the "second circuit means" is not found in the lock-step design taught by McDonald et al. '823.

Nothing in claim 26 requires data to be "indirectly" supplied to the second processor means, or precludes "direct" connection of the second processor to the memory.

Figure 4 of McDonald shows a first bus 7 coupling the memory means 24 to the first subprocessor unit 26 for communicating address and data signals therebetween, a first circuit means in the form of a driver/receiver 30, including second bus 15-1, coupling the first bus 7 to the second subprocessor unit 29 for communicating to the second subprocessor unit 29 data signals from the first bus means in a manner emulating the memory means to the second subprocessor unit. Appellants' contentions to the contrary notwithstanding, the "emulating" or imitation of one system with another system does not require that the operation of the imitating system lag the operation of the imitated system.

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The act of emulation² can occur in real time as in McDonald, or in lag time. In Figure 4 of McDonald, the second circuit means includes the driver 44 and bus 10-4 (coupled to the first circuit means via the first subprocessor unit 26), address comparator 6-4 which receives the address signals on bus 10-4, bus 11-4 which transfers address signals from the second subprocessor unit 29 to the address comparator 6-4, bus 10-1 (coupled to the first circuit means via bus 15-1) to transfer data signals from the first subprocessor unit 26 to a data comparator 6-1, and a bus 11-1 which transfers data signals from the second subprocessor unit 29 to the data comparator 6-1. Any "miscompare" from the comparators 6-1 and 6-4 will cause error signals to be generated on outputs 51 and 58, respectively.

The obviousness rejection of claim 26 is sustained because the contested limitations (i.e., the first and second

² Emulation is defined in the attached excerpts from the Encyclopedia of Computer Science, Ralston (Editor), pages 535, 925, 927 and 928 (New York, Van Nostrand Reinhold Company, 1976).

circuit means³) are found in the teachings of McDonald. In view of the grouping of the claims (Brief, pages 4 and 5), the obviousness rejection of claims 27 and 28 is likewise sustained.

Turning to claim 31, the lock-step operation in McDonald precludes "temporarily holding each instruction of the instruction stream before communicated to the second processor unit." Thus, the obviousness rejection of claims 31 through 33 is reversed because we agree with the appellants that "McDonald et al. specifically teaches lock step operation of pairs of CPUs," and that "[t]his is not what claim 31 specifies" (Brief, page 9).

Claims 35 and 36 require that the data or instruction words be provided to one digital circuit, and that the data or instruction words be provided to another digital circuit "at least one clock period after" or during "subsequent" clock periods. The claimed lagging operation is opposite to the

³ Appellants have not relied on the 6th paragraph of 35 U.S.C. § 112 to distinguish the claimed invention over McDonald, and have not rebutted the examiner's finding of equivalence (Answer, pages 8 and 9) between the claimed means for "emulating" and the structure found in McDonald.

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lock-step operation of the subprocessors in McDonald. Zieve was cited by the examiner to show two processors "operating in response to their independent clocks" (Answer, page 6). Although Zieve is capable of inserting a special function "at selected intervals to delay the lead processor until the other catches up" (column 1, lines 58 through 62), this special function is merely incidental to the simultaneous operation of the two processors (column 1, lines 55 through 58). The obviousness rejection of claims 35 and 36 is, therefore, reversed because Zieve can not cure the shortcomings in the teachings of McDonald.

DECISION

The decision of the examiner rejecting claims 26 through 28, 31 through 33, 35 and 36 under 35 U.S.C. § 103 is affirmed as to claims 26 through 28, and is reversed as to claims 31 through 33, 35 and 36. Accordingly, the decision of the examiner is affirmed-in-part.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
)	
)	
)	BOARD OF PATENT
ERROL A. KRASS)	APPEALS AND
Administrative Patent Judge)	INTERFERENCES
)	
)	
LEE E. BARRETT)	
Administrative Patent Judge)	

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Townsend and Townsend and Crew
Two Embarcadero Center
Eighth Floor
San Francisco, CA 94111