

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte KARL M. GUTTAG, KEITH BALMER, ROBERT J. GOVE,  
CHRISTOPHER J. READ, JEREMIAH E. GOLSTON, SYDNEY W. POLAND,  
NICHOLAS ING-SIMMONS and PHILIP MOYSE

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Appeal No. 1996-3391  
Application No. 08/160,573<sup>1</sup>

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ON BRIEF

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Before HAIRSTON, KRASS, and HECKER, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 37, constituting all the claims in the application.

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<sup>1</sup> Application for patent filed November 30, 1993.

The invention is directed to a data processing apparatus having an arithmetic logic unit (ALU) with three separate multibit digital inputs. The ALU performs mixed arithmetic and Boolean operations on the three inputs, wherein at least one of the mixed arithmetic and Boolean combinations performs a Boolean function prior to an arithmetic function. A shifter is connected to one of the three inputs for shifting the digital signal received at that input. A mask generator is also provided which generates a multibit digital mask signal as one of the three inputs to the ALU. A function control input to the ALU determines which operations will be performed on the three multibit digital inputs received by the ALU.

Representative independent claim 1 is reproduced as follows:

1. A data processing apparatus comprising:

an arithmetic logic unit having first, second and third data inputs for multibit digital signals representing corresponding first, second and third input signals, and a function control input signal for receiving a function signal, said arithmetic logic unit generating at an output a multibit digital signal representing a mixed arithmetic and Boolean combination of said first, second and third inputs corresponding to said function signal, said mixed arithmetic

and Boolean combination including at least one combination performing a Boolean function prior to an arithmetic function;

a first data source supplying a first multibit digital signal to said first data input of said arithmetic logic unit;

a second data source supplying a second multibit digital signal;

a shifter having a data input connected to said second data source, a shift control input receiving a shift control signal, and a data output connected to said second data input of the arithmetic logic unit, said shifter shifting said second multibit digital signal an amount corresponding to said shift control signal and supplying said shifted second multibit digital signal to said second data input of said arithmetic logic unit;

a third data source supplying a third multibit digital signal to said third data input of said arithmetic logic unit.

The examiner relies on the following references:

Chu et al. (Chu) 1988	4,785,393	Nov. 15,
Ing-Simmons et al. 1993	5,239,654	Aug. 24,
Ing-Simmons		(filed Nov. 17, 1989)

Claims 1 through 37 stand rejected under 35 U.S.C. 103 as unpatentable over Ing-Simmons in view of Chu.

Reference is made to the briefs and answer for the respective positions of appellants and the examiner.

OPINION

We have carefully reviewed the evidence before us, including, inter alia, the references to Ing-Simmons and Chu in addition to the arguments of appellants and the examiner and, as a result of such a review, we will sustain the rejection of claims 1 through 3, 5 through 14 and 16 through 37 under 35 U.S.C. 103 but we will not sustain the rejection of claims 4 and 5 under 35 U.S.C. 103.

As a general proposition in an appeal involving a rejection under 35 U.S.C. 103, an examiner is under a burden to make out a prima facie case of obviousness. If that burden is met, the burden of going forward then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223

USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976).

We now consider the rejection of independent claims 1 and 12 as unpatentable over Ing-Simmons and Chu. In accordance with appellants' grouping, at page 4 of the principal brief, claims 5 through 8, 10, 11, 16 through 19 and 21 through 37 will stand or fall with the independent claims and independent claim 12 will stand or fall with independent claim 1. Accordingly, we consider the rejection of claim 1.

At page 4 of the final rejection (Paper No. 4), the examiner has set forth the rationale for the rejection, particularly pointing out that Chu discloses a three-input ALU consisting of two data operands and a mask with the Chu apparatus executing three operand instructions with masking for any function. The examiner also points out that Chu shows a shifter for the R input to the ALU and a shifter for the mask.

Appellants argue that the combination of Ing-Simmons and Chu does not disclose the claimed

said arithmetic logic unit generating at an output a multibit digital signal representing a mixed arithmetic and Boolean combination of said first, second and third inputs corresponding to said function signal, said mixed arithmetic and Boolean combination including at least one combination performing a Boolean function prior to an arithmetic function.

While Ing-Simmons may not disclose this feature, in our view, Chu clearly does. Even appellants admit, at page 4 of the principal brief, that Figure 12 of Chu "clearly shows that ALU 130 consists of arithmetic logic unit block 496 and 2:1 multiplexer 494" and that Chu "clearly forms the three input combination with an arithmetic/logical combination of the R and S inputs formed first in arithmetic logic unit operation block 496 and the Boolean/mask combination formed in 2:1 multiplexer 494 according to the M input." Thus, there is no question that Chu discloses an ALU and a multibit digital signal representing a mixed arithmetic and Boolean combination of the first, second and third inputs corresponding to a function signal. The only issue seems to revolve around whether Chu suggests that the mixed arithmetic and Boolean combination includes "at least one combination performing a Boolean function prior to an arithmetic function."

Referring to Chu's Figure 12, appellants argue that this figure shows that the only way that the ALU of Chu can form a mixed arithmetic and Boolean combination of three inputs "is by first forming an arithmetic combination of the R and S inputs and then masking this according to the M input." This, contend appellants, is in the opposite order required by the claims, wherein a Boolean function is performed "prior to an arithmetic operation."

We find appellants' argument in this regard to be unpersuasive. First, even assuming, arguendo, that appellants are correct in their assessment, and that Chu discloses only one order of operation, i.e., arithmetic combination followed by a Boolean operation, since appellants have shown no criticality to the specific order of operations, the skilled artisan would have understood, and found obvious, that, without a showing to the contrary, the order of operations performed should have no bearing on the final result, as in  $A + B = B + A = C$ . Now, we understand that this associative law may only apply to simple additive and subtractive operations and not to operations involving, say, addition and multiplication since A

$+(B \times C)$  would not, necessarily, equal  $(A + B) \times C$ . However, the broad language of the instant claims does not specify any particular arithmetic function or any particular Boolean function.

In any event, we find appellants' argument to be unpersuasive because the argument is based solely on Chu's Figure 12 which shows an ALU operation being performed on R and S, and then the Boolean function being performed in the 2:1 multiplexer after the arithmetic combination. However, when Chu describes Figures 13A and 13B, at the bottom of column 46, Chu indicates that although the 2:1 multiplexer 494 is shown on the exterior of ALU operation block 496 in Figure 12, that multiplexer, which performs the Boolean operation, may be "incorporated within each of the NLC 500a-500p" which are shown as being within ALU operation block 496 in Figures 13A and 13B. Therefore, appellants' argument that Chu shows only the order wherein the arithmetic combination is performed first, followed by the Boolean function, is not entirely correct. Since Chu suggests that the elements for performing both the Boolean function and the arithmetic combination may be within the same

ALU operation block 496, and lines 54-56 of column 46 of Chu discloses that the signals on the R and S-operand inputs of the ALU are "used to perform the arithmetic and/or logic operations..." this would appear to suggest that, indeed, there would be no fixed order of operation between the Boolean functions and the arithmetic combinations.

Thus, in our view, the examiner has established a prima facie case of obviousness, with regard to independent claims 1 and 12, which has not been overcome by any objective evidence or arguments presented by appellants. Accordingly, we will sustain the rejection of claims 1, 5 through 8, 10 through 12, 16 through 19 and 21 through 37 under 35 U.S.C. 103.

Turning now to claims 2, 3, 13 and 14, claims 2 and 13 recite that the shifter performs a right shift or a left shift based on the digital state of a predetermined bit of the shift control signal. Claims 3 and 14, depending from claims 2 and 13, respectively, recite that the predetermined bit is the most significant bit of the shift control signal. At pages 4-5 of the final rejection (Paper No. 7), the examiner has provided a

reasonable analysis as to why the shift control, as broadly recited in the claims, would have been obvious to the artisan in view of the applied prior art. Appellants argue that Ing-Simmons fails to provide for such a shift control and they further argue, with regard to Chu, that Chu "clearly shows that control of additional structures, namely source mux 136 and swap mux 138, are required for control of whether the shift is left or right" [principal brief-page 9]. As broadly claimed, it matters not from where the control signal comes and, in our view, the artisan would have found it obvious to apply either a data signal or a control signal to the shift control input of the Chu shifter. Whatever controls the direction and amount of shift in Chu can be considered as the claimed shift control input. Further, the artisan would have found it obvious that any bit at the shift control input can be the directional control bit, including the most significant bit. Accordingly, we will sustain the rejection of claims 2, 3, 13 and 14 under 35 U.S.C. 103.

We now turn to claim 9, with which claim 20 stands or falls. Claim 9 depends from claim 1 and recites that a

plurality of data registers receives an input from the output of the ALU and an input from the output of the shifter. At pages 5-6 of the final rejection (Paper No. 7), the examiner has provided a reasonable analysis as to why the presence of registers, as broadly recited in claim 9, would have been obvious to the artisan in view of the applied prior art. Appellants contend that claim 9 requires both storage of the shifter output in a data register and storage of the output of the ALU in a data register. Appellants then point to instant Figure 5 to illustrate a "connection" from barrel rotator 235 via Bmux 227 and multiplier destination bus 203 to data registers 200. Appellants then argue that neither Ing-Simmons nor Chu discloses the particular connection between the output of the data registers and the plurality of data registers recited in claim 9.

We agree with the examiner's response, at pages 12-13 of the answer, to appellants' arguments. Clearly, Chu discloses a shifting and an output of the ALU is fed to a register (see Figure 1 of Chu). We agree with the examiner [answer-page 13] that "shifting amount and direction is dependent upon the

particular application... It would have been obvious...to tailor shifting mechanisms to the particular application."

Accordingly, we will sustain the rejection of claims 9 and 20 under 35 U.S.C. 103.

Finally, we turn to the rejection of claim 4, with which claim 15 will stand or fall. Claim 4 spells out, in detail, a data register file and its connections to the ALU. Here, while the examiner initially appears to have presented a reasonable analysis [answer-pages 5-6] with regard to the rejection of claim 4 under 35 U.S.C. 103, upon further analysis we find the rejection lacking and will not sustain it or the rejection of claim 15 under 35 U.S.C. 103.

The examiner says that Ing-Simmons discloses a variety of data registers including a data register file and a register destination (via Mux element 3309) to store the output of the ALU. Further, Chu discloses the use of registers in Figure 1 and it is well known to use registers as temporary storage devices. While, at first blush, the examiner's comments seem

reasonable, claim 4 calls for more. In response to the examiner's rejection, appellants contend that Ing-Simmons fails to disclose that the shift control input comes from a data register. While appellants do admit that, "at best," Ing-Simmons suggests that the shift amount is stored in OPTIONS register 3310, appellants contend that this OPTIONS register is separate from data register file 3300 [principal brief-page 10]. The examiner [at pages 10-11 of the answer] contends that by specifying one register as a "special function data register," this reasonably implies that the register is used for the purpose of storing the shift amount and is not a general purpose data register. Therefore, one could interpret this special function data register as being distinct from other registers in the register file. Accordingly, Ing-Simmons' OPTIONS register may be considered a "special function data register," as set forth in the claim. However, as pointed out by appellants [reply brief-page 5], claim 4 specifically requires that the "special function data register" which stores a default shift amount, must be "a predetermined one of said plurality of data registers." Therefore, the examiner's interpretation that the "special function data register" may be

distinct from other registers in the register file does not comport with a fair interpretation of the specific claim language. Accordingly, we will not sustain the rejection of claims 4 and 15 under 35 U.S.C. 103.

We have sustained the rejection of claims 1 through 3, 5 through 14 and 16 through 37 under 35 U.S.C. 103. We have not sustained the rejection of claims 4 and 15 under 35 U.S.C. 103. Accordingly, the examiner's decision is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR 1.136(a).

AFFIRMED-IN-PART

KENNETH W. HAIRSTON	)	
Administrative Patent Judge	)	
	)	
	)	
	)	
	)	BOARD OF PATENT
ERROL A. KRASS	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
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STUART N. HECKER	)	
Administrative Patent Judge	)	

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Application No. 08/160,573

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