

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte LARRY L. BYERS

Appeal No. 96-3274
Application 08/173,408¹

ON BRIEF

Before JERRY SMITH, BARRETT, and BARRY, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from

¹ Application for patent filed December 23, 1993, entitled (as amended by Paper No. 5) "Method And Apparatus For Asynchronous Device Communication."

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the final rejection of claims 1-10 and 15. The amendment after final rejection to claim 6 (Paper No. 17) has been entered.

We reverse.

BACKGROUND

The disclosed invention is directed to a data interface among micro-engines. A "micro-engine is a specialized controller incorporating customized random logic within a basic micro-code processor" (specification, page 4). The micro-engines are attached via a point-to-point interface to a Network Interface Module (NIM) (i.e., there is no communication among all the system components). The NIM provides normal system level control of the major system components and contains the synchronization circuitry to provide asynchronous timing between the NIM and a dynamic register in the micro-engine.

Claim 1 is reproduced below.

1. In a digital data processing system having a system element embedded in a parallel processing architecture, an apparatus comprising:

- a. a micro-engine for controlling said system element;

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- b. a register located within and directly addressable by said micro-engine; and
- c. a network interface module, having a point-to-point interface, which is timed asynchronously with respect to said micro-engine and which is coupled to said register through said point-to-point interface whereby said network interface module writes into and reads from said register through said point-to-point interface.

The examiner relies on the following prior art patent:

Petersen et al. (Petersen) 5,299,313 March 29,
1994

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Claims 1-10 and 15 stand rejected under 35 U.S.C. § 103 as being unpatentable over Petersen.

We refer to the Final Rejection (Paper No. 6) (pages referred to as "FR__") and the Examiner's Answer (Paper No. 18) (pages referred to as "EA__") for a statement of the Examiner's position and to the Appeal Brief (Paper No. 14) (pages referred to as "Br__") for a statement of Appellant's arguments thereagainst.

OPINION

With respect to claim 1, Appellant argues only that Petersen does not disclose (1) a network interface module that is timed asynchronously with respect to a micro-engine, and (2) a point-to-point interface. Apparently, it was agreed that Petersen shows all the claimed limitations except for these two features (Examiner Interview Summary Record, Paper No. 7). However, we have trouble understanding the whole of the Examiner's rejection.

The Examiner finds the "micro-engine for controlling said system element" to correspond to the "host interface logic 102" mentioned at column 9, line 48 (EA3). The Examiner finds the "register located within and directly addressable by

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said micro-engine" to correspond to the "adapter interface host address space [101]" in figures 3 and 4, described at column 10, lines 37-45, and column 24, line 14 (EA3). The Examiner finds the "network interface module" to correspond to the "network interface logic 104" mentioned at column 10, line 3 (EA3). The flow diagram for these elements is shown in figure 3 of Petersen.

We see several problems with the rejection. First, the Examiner does not identify what element in Petersen corresponds to the "system element embedded in a parallel processing architecture" which is controlled by the micro-engine. We assume that the Examiner has ignored the preamble limitation of "in a parallel processing architecture," although this is not stated. It is difficult to tell how the "host interface logic 102" can be considered to "control" anything since its modules 107, 108 merely "manage communication of data between the independent memory 103 and the host in response to writes by the host system to the adapter interface address block 101" (col. 9, lines 65-68).

Second, the registers pointed to by the Examiner are in

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the adapter interface host address space 101 and the network interface logic does not have access to this address space. Perhaps the Examiner meant to refer to the registers in the adapter's memory 103 (e.g., col. 11, lines 6-10).

Third, both the host interface logic 102 and the network interface logic 104 in figure 3 are part of the network interface processor 14 in figure 1; the functional units of the network interface processor are shown in figure 2. It appears as if the Examiner has divided the network interface processor 14, which seems to best correspond to a "network interface module," into both a "micro-engine" and a "network interface module." We would have liked to see some reasoning for this interpretation.

Nevertheless, since Appellant argues only that Petersen does not disclose a network interface module that is timed asynchronously with respect to a micro-engine, and a point-to-point interface, we limit our analysis to those two differences. The Examiner admits that Petersen does not disclose asynchronous timing or a point-to-point interface (FR3).

Regarding the asynchronous timing limitation, the

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Examiner concludes (FR3-4):

[I]t would have been obvious to one of ordinary skill in the art at the time of invention to provide such arrangement in Peterson's [sic] system because it would have allowed the network interface module to operate asynchronously with respect to the micro-engine, thereby eliminating the use of [a] synchronous clock which otherwise might have been needed during the synchronous operation of the network interface module and the micro-engine.

We find no factual support for the Examiner's reasoning. The Examiner seems to say that it would have been obvious to provide asynchronous timing so that the system can operate asynchronously. This does not address the question of why one of ordinary skill in the art would have been motivated to use asynchronous timing in the closely coupled system of Petersen where the host interface logic 102 and the network interface logic 104 are part of the same network interface processor 14. The Examiner has made up a reason to account for the difference and has not attempted to back up the conclusion by pointing to support in Petersen or in the knowledge of those of ordinary skill in the art. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification."

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In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992), citing In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). We agree with Appellant's arguments that the Examiner's rejection is based on Appellant's disclosure.

With respect to the point-to-point interface limitation, the only reasoning we find by the Examiner regarding the point-to-point interface limitation is the following (FR4; EA8):

[T]he point-to-point interface would have allowed the system to efficiently support asynchronous communication and would have also allowed direct communication between the various elements of the system.

Again, we find no factual support for the Examiner's reasoning. The Examiner seems to say that the point-to-point interface would be advantageous for an asynchronously timed system, but the Examiner has not attempted to back up the conclusion by pointing to support in Petersen or in the knowledge of those of ordinary skill in the art. We agree with Appellant's arguments that the Examiner's rejection appears to be based on Appellant's disclosure. Nevertheless, under the Examiner's interpretation of Petersen, where the host interface logic 102 is the "micro-engine," the "register"

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is in adapter memory 103 (in RAM 50), and the network interface logic 104 is the "network interface module," it appears that the RAM interface 50 constitutes a point-to-point interface between the network interface logic 104 and the register. Appellant argues that Petersen does not have a point-to-point interface because it has a bussed architecture (Br25). However, the network interface logic 104 does not use the EISA bus. Therefore, although this teaching of Petersen is not appreciated by the Examiner, it appears that Petersen does have a point-to-point interface. Moreover, it seems that a bus can be said to broadly provide a point-to-point interface between two elements on the bus.

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In conclusion, the Examiner has failed to establish a prima facie case of obviousness with respect to the "timed asynchronously" limitation of claim 1. The rejection of claim 1 and its dependent claims 2-4 is reversed. Independent claims 5-7 and 15 also require asynchronous timing and, hence, the rejection of claims 5-10 and 15 is likewise reversed.

REVERSED

JERRY SMITH)	
Administrative	Patent Judge)
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)	BOARD OF PATENT
LEE E. BARRETT)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
)	
)	
LANCE LEONARD BARRY)	
Administrative Patent Judge)	

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NAWROCKI, ROONEY & SIVERTSON
3433 Broadway Street Northeast
Broadway Place East
Suit 401
Minneapolis, MN 55413