

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 23

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CIARIN B. CLOSE, RICHARD A. GAHAN and BRYAN T. CAMPBELL

Appeal No. 1996-3095
Application 08/346,311¹

ON BRIEF

Before THOMAS, HAIRSTON, and FRAHM, Administrative Patent Judges.

FRAHM, Administrative Patent Judge.

DECISION ON APPEAL

Appellants have appealed to the Board from the examiner's final rejection of claims 1 to 4,

¹ Application for patent filed November 28, 1994. According to appellants, this application is a continuation of Application 07/818,611 filed January 10, 1992, now abandoned.

which constitute all of the pending claims in the application before us.

BACKGROUND

The subject matter on appeal is directed to a DRAM parity protection scheme which uses horizontal and vertical parity bits to detect and correct soft errors in the memory (see specification, page 1). As stated by appellants at pages 1 to 2 of the specification, soft errors caused by alpha particles emitted from within the DRAM can change bit data from one logic level (e.g., "1") to another (e.g., "0"). By performing parity checking using parity bits which are located in a protected memory space which is a subset of, and separate from, the total DRAM space used for data storage, appellants have overcome difficulties of prior art parity protection schemes. Appellants' DRAM parity protection scheme of claims 1 to 4 on appeal enables soft error correction using parity checking which provides the significant improvement of restarting of the code while avoiding completely reloading the code (see specification, page 3).

Representative independent claim 1 is reproduced below:

1. A DRAM memory comprising:

a plurality of memory storage cells arranged in an array of rows and columns;

a protected memory space comprising a subset of the rows and the columns of memory storage cells wherein data and horizontal parity bits for the data are stored, and a vertical parity database wherein vertical parity bits are stored;

the data stored in the protected memory space being arranged in rows of horizontally contiguous bytes;

the vertical parity bits being arranged in a row separate from the rows of horizontally contiguous bytes of data;

each of the vertical parity bits relating to a corresponding one of the subset set of columns in which at least one bit of data is stored;

each of the vertical parity bits being generated from the data stored in the corresponding column of data to which the vertical parity bit relates, and each of the vertical parity bits reflecting parity of the corresponding column of data;

wherein at least one byte of the data is accessed by an address and checked for horizontal parity;

wherein when the horizontal parity of at least one of the bytes shows an error exists, a row location of the error is determined by the address and a vertical parity check is run for the at least one of the bytes addressed to determine a column location of the error, the row location and the column location defining a particular bit location of the error.

The following reference is relied on by the examiner:

| | | |
|-------|-----------|--------------|
| Osman | 4,453,251 | Jun. 5, 1984 |
|-------|-----------|--------------|

Claims 1 to 4 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon Osman alone.

Rather than repeat the positions of appellants and the examiner, reference is made to the Briefs and the Answer for the respective details thereof.²

OPINION

In reaching our conclusion on the issues raised in this appeal, we have carefully considered

² We note that the Reply Brief submitted December 4, 1995, was apparently entered and considered by the examiner, and will be treated by us as part of the record for purposes of this opinion.

appellants' specification and claims, the applied patent, and the respective viewpoints of appellants and the examiner. As a consequence of our review, we are in general agreement with appellants (Brief, pages 4 to 6; Reply Brief, pages 1 to 4) that the claims on appeal would not have been obvious to one of ordinary skill in the art at the time the invention was made in light of the collective teachings of Osman. We find that the examiner has failed to make out a prima facie case of obviousness. For the reasons which follow, we will not sustain the decision of the examiner rejecting claims 1 to 4 under 35 U.S.C. § 103.

Appellants argue (Brief, page 4; Reply Brief, pages 3 to 4) that Osman neither taught nor would have suggested parity bits being stored in a separate row of memory cells (i.e., one which does not include data bits). We agree with appellants that in Osman "there are no parity bits, vertical or horizontal, that are stored in a separate row of memory cells, i.e., a row that does not also include data bits" (Reply Brief, page 3). Representative claim 1 on appeal calls for:

a protected memory space comprising a subset of the rows and the columns of memory storage cells wherein data and horizontal parity bits for the data are stored, and a vertical parity database wherein vertical parity bits are stored;

the data stored in the protected memory space being arranged in rows of horizontally contiguous bytes;

the vertical parity bits being arranged in a row separate from the rows of horizontally contiguous bytes of data;

We find that claim 1 on appeal requires that the vertical parity bits are in a protected memory space which is required to be separate from the data bits stored in the DRAM. We also find that Osman

"does not disclose the storage of vertical parity bits in a row separate from the rows in which data is stored" (Brief, page 4). Specifically, we find that Osman discloses (see Figure 3 and the accompanying text at column 3) that "data bits are stored in all of the memory cells that lie in columns C_1 through C_N in arrays A_1 through A_x ," and "parity bits are stored in all of the remaining memory cells" (column 3, lines 44 to 47). Because we agree with appellants that no parity bits are stored in a row that does not also include other data, we will reverse the decision of the examiner rejecting claims 1 to 4 under 35 U.S.C. § 103.

Appellants correctly state that the examiner admits that "[n]ot particularly taught by Osman is that one's memory space is a subset of a larger memory space" (Answer, page 4). We agree that such a feature of a protected memory space is neither taught nor would have been suggested by Osman. We cannot agree with the examiner's circular reasoning that "the largest subset of a set is the set itself; therefore, the partitioning of data locations into sets does not distinguish the invention" or that "the grouping of data into subsets is well known" (Answer, page 4). The examiner has provided no reference teaching or suggestion for such a proposition. Accordingly, we find that the examiner has failed to make a prima facie case that the collective teachings and/or suggestions of Osman would have taught or suggested the protected memory space having separate vertical parity rows as claimed in claim 1 on appeal.

In light of the foregoing, the differences between the subject matter recited in the claims and the

Appeal No. 1996-3095
Application 08/346,311

reference are such that the claimed subject matter as a whole would not have been obvious within the meaning of 35 U.S.C. § 103. Accordingly, we will not sustain the rejection of claims 1 to 4 on appeal.

CONCLUSION

The decision of the examiner rejecting claims 1 to 4 under 35 U.S.C. § 103 is reversed.

REVERSED

| | | |
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| JAMES D. THOMAS |) | |
| Administrative Patent Judge |) | |
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| |) | |
| |) | |
| KENNETH W. HAIRSTON |) | BOARD OF PATENT |
| Administrative Patent Judge |) | APPEALS AND |
| |) | INTERFERENCES |
| |) | |
| |) | |
| ERIC FRAHM |) | |
| Administrative Patent Judge |) | |

Appeal No. 1996-3095
Application 08/346,311

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