

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

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Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte HENG S. HUANG

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Appeal No. 96-2940  
Application 08/259,073<sup>1</sup>

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ON BRIEF

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Before BARRETT, FLEMING, and GROSS, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

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<sup>1</sup> Application for patent filed June 13, 1994, entitled "Process For Producing Very Narrow Buried Bit Lines For Non-Volatile Memory Devices."

Appeal No. 96-2940  
Application 08/259,073

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1-25.

We reverse.

#### BACKGROUND

The disclosed invention is directed to a process for forming very narrow closely spaced buried bit lines.

Claim 18 is reproduced below.

18. A method of forming a plurality of self-aligned closely spaced very narrow buried conductive lines in a semiconductor substrate, comprising the steps of:

providing a thin insulating layer on the surface of the semiconductor substrate,

forming masking stripes having vertical sidewalls over the thin insulating layer,

forming polysilicon spacers on the vertical sidewalls of the masking stripes,

forming a glass layer between the spacers,

preferentially etching the polysilicon spacers forming narrow openings between the masking lines and the glass layer, and

implanting impurity ions into said substrate through the narrow openings to form conductive buried lines.

The Examiner relies upon the following prior art:

Appeal No. 96-2940  
Application 08/259,073

Jun et al. (Jun) 1993	5,256,587	October 26,
Hsue et al. (Hsue) <sup>2</sup> 10, 1994	5,310,693	May

Wolf, S., Silicon Processing for the VLSI Era, Volume 1 - Process Technology, Lattice Press (1986), pp. 285, 286, 290.

Claims 1-25 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hsue, Wolf, and Jun. Wolf appears to be relied on only for the rejection of claims 8, 22, and 25.

We refer to the Final Rejection (Paper No. 4) and the Examiner's Answer (Paper No. 9) (pages referred to as "EA\_\_") for a statement of the Examiner's position and to the Brief (Paper No. 8) (pages referred to as "Br\_\_") for a statement of Appellant's position.

OPINION

Claim 18 is broader than claim 1 and is taken as the representative claim. The selection of claim 18 rather than claim 1 does not affect the merits of the decision because the contested limitations are present in both claims.

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<sup>2</sup> In the Examiner's Answer, the Examiner cites Hsue, U.S. Patent 5,310,693, issued May 10, 1994. After some confusion, we discovered that the Examiner meant Hsue et al., U.S. Patent 5,318,921. The Examiner should be more careful in citing the references relied on in the future.

Appeal No. 96-2940  
Application 08/259,073

Appellant argues four differences over Hsue (Br9):

(1) the claims call for a glass layer between spacers as opposed to Hsue which uses a thermal oxide, which is said to provide a thicker mask allowing for more etch process tolerance and the glass does not add thermal stress to the chip as does Hsue's thermal oxide process; (2) the claims call for polysilicon spacers as opposed to Hsue's nitride spacers, which is said to not add stress like nitride spacers; (3) the disclosed silicon oxide insulating layer under the polysilicon foundation layers which allows the use of a one step etch to remove the polysilicon spacers, the foundation layer, and the insulating layer in the opening as opposed to Hsue which has a nitride insulating layer and uses a three step etch; and (4) the disclosed one step spacer etch as opposed to Hsue's three step etch, which is said to have the advantage of being simpler and less expensive.

We find that argued differences (3) and (4) are not commensurate in scope with independent claim 18 or independent claim 1 because these claims do not recite the material used for the insulating layer, nor do they recite a one-step etching process. This is discussed by the Examiner at EA6.

Appeal No. 96-2940  
Application 08/259,073

Therefore, only the argued differences (1) and (2) are relevant.

Hsue does exactly what Appellant does in terms of a process using sidewalls to form closely spaced bit lines and word lines. Hsue notes (col. 1, lines 18-21): "Researches in the integrated circuit field generally have used the sidewall technology to form smaller spaces than normally available through lithography for various purposes." Appellant's claims 1-25 are directed to a process wherein different materials are used for the layer between sidewall spacers, difference (1), and for the sidewall spacers, difference (2); that is, claim 18 would be anticipated by Hsue if the terms "polysilicon" and "glass" were not present. One of ordinary skill in the semiconductor art doubtless would have appreciated that different materials and process steps could be used to form the layer between sidewalls and the sidewalls. The issue here is whether the Examiner has established that a person of ordinary skill in the art would have been led to substitute the claimed materials from Jun.

The Examiner relies on Jun for differences (1) and (2). Jun discloses depositing a layer of polysilicon 3 in a

Appeal No. 96-2940  
Application 08/259,073

temperature range "about the transition temperature at which the deposited polysilicon transitions from being deposited in an amorphous form to being deposited in a polycrystalline form" (col. 3, lines 24-27). "Formation of the polysilicon layer a [sic] described above results in a layer consisting of raised, rounded polysilicon features generally resembling 'hemispheres,' with characteristics of the hemispheres such as size, shape and pitch dependent upon the particular deposition conditions." Col. 3, lines 27-32. As shown in the figure 4 embodiment, the hemisphere particle layer 14 has alternating hills and valleys. "On hemisphere particle layer 14, planarizing insulation layer 15 of a material having an etching selectivity higher than that of polysilicon is coated. The material of planarizing insulation layer 15 may be SOG [spin on glass], polyamide, CVD oxide or CVD nitride." Col. 4, lines 63-67. The layer 15 is etched back to expose the crest of each hill. "Thereafter, the exposed hill portions of hemisphere particle layer 14 are etched back by using remaining portions of layer 15 as a pattern mask." Col. 5, lines 4-6.

Appeal No. 96-2940  
Application 08/259,073

The Examiner's position is as follows (EA4-5):

It would have been obvious to one of ordinary skill in the art to have substituted the steps of forming a planarizing oxide layer followed by etchback over the sacrificial spacers for the step of forming thermal oxide between the spacers in the process of Hsue since Jun et al teach such a process as appropriate for exposing sacrificial spacers between oxide in a narrow mask forming process such as that of Hsue.

It further would have been obvious to have formed conformal polysilicon and then polysilicon sacrificial spacers instead of nitride spacers in the process of Hsue since Jun et al teach polysilicon spacers as being an appropriate sacrificial spacer material when etched between oxide lines.

We are not persuaded by the Examiner's reasoning because we find no good explanation of why one of ordinary skill in the semiconductor art would have sought to use the glass and polysilicon teachings of Jun in the environment of Hsue without using Appellant's teachings as a guide. Hsue does not suggest substitute materials for the silicon nitride sidewall spacers or for the silicon oxide layer between spacers, although we have no doubt that one skilled in the art would have recognized that other materials and processes could have been used. Jun does not disclose sidewall spacers or implantation of impurity ions and does not resemble Hsue in any way identified by the Examiner such that its construction

Appeal No. 96-2940  
Application 08/259,073

materials would naturally suggest the use of Jun's materials in Hsue. The Examiner has apparently used the claimed glass layer and polysilicon sidewall spacers as the reason for looking for a reference with polysilicon being masked by glass. This is hindsight. A showing of recognized equivalence between polysilicon and silicon nitride as sidewalls spacers and a showing of recognized equivalence between glass and thermally formed silicon dioxide as a masking layer would have been persuasive, but merely finding glass and polysilicon in some semiconductor environment is not. In our opinion, the Examiner has failed to establish a prima facie case of obviousness. The rejection of claims 1-25 is reversed.

REVERSED

LEE E. BARRETT )  
Administrative Patent Judge )  
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 ) BOARD OF PATENT

Appeal No. 96-2940  
Application 08/259,073

MICHAEL R. FLEMING	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
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ANITA PELLMAN GROSS	)	
Administrative Patent Judge	)	

Appeal No. 96-2940  
Application 08/259,073

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