

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JIMMIE D. CHILDERS,
SEIICHI YAMAMOTO and
MASANARI TAKEYASU

Appeal No. 96-2820
Application 08/227,705¹

ON BRIEF

Before KRASS, FLEMING and HECKER, **Administrative Patent
Judges.**

HECKER, **Administrative Patent Judge.**

DECISION ON APPEAL

¹ Application for patent filed April 14, 1994. According to appellants,
this application is a continuation of 07/918,161, filed July 21, 1992, which
is a continuation of Application 07/486,984, filed March 01, 1990.

This is a decision on appeal from the final rejection of claims 81 through 90, all of the claims pending in the present application. Claims 1 through 80 have been canceled.

The invention relates to a processor having a plurality of processing elements. In particular, Appellants disclose on page 17 et seq. of the specification and illustrate in Figure 4 a processing element 20(n). Each processor element 20(n) has an input register 11 of M rows, a first memory bank 12 of J rows (wherein J does not equal M), a first sense amplifier 40, an ALU 13, an output register 16 of L rows, a second memory bank 15 of J rows and a second sense amplifier 42. The first sense amplifier 40 is shared between the input register 11 and the first memory bank 12. The second sense amplifier 42 is shared between the output register 16 and second memory bank 15.

Representative independent claim 81 is reproduced as follows:

81. Storage circuitry comprising:

a first memory having a plurality of M rows of first memory cells, each of said first memory cells connected to a first pair of bit lines;

a set of M first word lines, each first word line connected to a corresponding one of said first memory cells;

a second memory having a plurality of J rows of second memory cells, where J does not equal M, each of said second memory cells connected to a second pair of bit lines;

a set of J second word lines, each second word line connected to a corresponding one of said second memory cells;
and

sense amplifier circuitry located between said first memory and said second memory and connected to said first pair of bit lines and said second pair of bit lines, said sense amplifier circuitry including

amplifier pair of a sense amplifier having a pair of sense bit lines and a pair of output lines, said sense amplifier producing an output signal on said output lines corresponding to a ratio of voltages on said pair of sense amplifier bit lines,

amplifier lines a first gate circuit selectively connecting said first pair of bit lines to said pair of sense bit lines or isolating said first pair of bit lines from said pair of sense amplifier bit lines, and

said lines, a second gate circuit selectively connecting said second pair of bit lines to said pair of sense amplifier bit lines or isolating said second pair of bit lines from said pair of sense amplifier bit lines,

whereby said sense amplifier circuitry produces said output signal a) corresponding to data stored in a first memory cell accessed by one of said first word lines when said first gate circuit connects said pair of bit lines to said pair of sense

Appeal No. 96-2820
Application 08/227,705

amplifier bit lines and said second gate circuit isolates said second pair of bit lines from said pair of sense amplifier bit lines, and b) corresponding to data stored in a second memory cell accessed by one of said second word lines when said first gate circuit isolates said first pair of bit lines from said pair of sense amplifier bit lines and said second gate circuit connects said second pair of bit lines to said pair of sense amplifier bit lines.

The Examiner relies on the following references:

Schutz et al. (Schutz)	4,584,672	Apr. 22, 1986
Miyabayashi et al. (Miyabayashi)	4,916,667	Apr. 10, 1990 (filed Dec. 20, 1988)
Sakui et al. (Sakui)	4,926,382	May 15, 1990 (filed Nov. 23, 1988)
Matsui et al. (Matsui)	4,931,994	June 5, 1990 (filed Feb. 16, 1988)
Childers	4,939,575	July 3, 1990 (filed Sept. 5, 1989)
Hannai	4,947,377	Aug. 7, 1990 (filed Apr. 15, 1988)

Claims 81 through 90 stand rejected under 35 U.S.C. § 112, first, second and sixth paragraphs. Claims 81, 83, 84, 86, 87 and 89 stand rejected under 35 U.S.C. § 103 as being unpatentable over Childers with any of Hannai or Miyabayashi or Schutz or Matsui. Claims 82, 85, 88 and 90 stand rejected under 35 U.S.C. § 103 as being unpatentable over Childers in

Appeal No. 96-2820
Application 08/227,705

view of any of Hannai or Miyabayashi or Schutz or Matsui, as applied to claims 81, 83, 84, 86, 87 and 89, and further in view of Sakui. Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the brief and answer for the respective details thereof.

OPINION

After a careful review of the evidence before us we will not sustain the rejection of claims 81 through 90 under 35 U.S.C. § 103 or 35 U.S.C. § 112.

Under the 35 U.S.C. § 112 rejection, the Examiner states that there is no support or inadequate support in the specification for the sense amplifiers (with pairs of inputs and outputs), addressing means, a commutator, dual port input's, arithmetic logic units (ALU's), a third word line, a dual port output register, an output commutator, second sense amplifier, gate circuits, and third and fourth amplifiers. The Examiner continues by stating that whatever is disclosed is "lacking sufficient description in the specification to enable a determination of the equivalency of the implicit and

Appeal No. 96-2820
Application 08/227,705

explicit claimed 'means'." (answer at page 3), and therefore not in compliance with 35 U.S.C. § 112 paragraph 6. On page 9 of the answer the Examiner states "Clearly all that is disclosed is a catch-all of intended functions without any real disclosure as to how to make and use these intended functions."

Appellants have responded by noting that the questioned "addressing means" has been changed to "word lines" making this point moot. Also, Appellants have identified support in the specification and figures for all other questioned items noted by the Examiner and recited in the claims. With regard to the adequacy of the specification, Appellants take the position that they "are not required to describe in detail elements known in the art", and cite prior art references that disclose further details (brief at the top of page 13).

We agree with the Appellants that their disclosure does provide support for the elements claimed, and find that the scope of the claim language does not exceed the support noted in the specification. Moreover, we have no problem with

Appeal No. 96-2820
Application 08/227,705

the specification with regard to "the equivalency of the implicit and explicit claimed 'means'" as argued by the Examiner. Thus, we will not sustain the rejection of the claims under 35 U.S.C.

§ 112 paragraphs 1, 2 and 6.

Turning to the rejections under 35 U.S.C. § 103, we find the Examiner has failed to set forth a *prima facie* case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the reasonable teachings or suggestions found in the prior art, or by a reasonable inference to the artisan contained in such teachings or suggestions. *In re Sernaker*, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983).

"Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." *Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.*, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), *citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), *cert. denied*,

Appeal No. 96-2820
Application 08/227,705

469 U.S. 851 (1984).

With regard to the rejection of claim 81, the Examiner holds that Childers teaches the claimed invention except for locating a sense amplifier between memories, and that any of Hannai or Miyabayashi or Schutz or Matsui teach the advantages of locating a sense amplifier between memories.

Reviewing claim 81 we note that the claim recites that the sense amplifier is located between two memories of different sizes, i.e. the "first memory having . . . M rows", and the "second memory having . . . J rows . . . , where J does not equal M, . . .". Reviewing the secondary references, we find that the sense amplifiers are always located between memories of the same size. Appellants urge that the secondary references would motivate one skilled in the art to dispose equal memories on the two sides of the sense amplifier to obtain the best average capacitance and sense times. Thus, Appellants urge, it would not be obvious to place a sense amplifier between memories of unequal size as claimed.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by

Appeal No. 96-2820
Application 08/227,705

the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." ***Para-Ordnance Mfg. v. SGS Importers Int'l***, 73 F.3d at 1087, 37 USPQ2d at 1239, ***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d at 1551, 220 USPQ at 311.

Even though Childers teaches memories of unequal size, it does not locate the sense amplifier between those memories. The secondary references teach locating a sense amplifier between memories of equal size to average the capacitance and speed sense times. The secondary references do not teach or suggest to one of ordinary skill in the art, to locate a sense amplifier between memories of unequal size. Since there is no evidence in the record that the prior art suggested the desirability of locating a sense amplifier

Appeal No. 96-2820
Application 08/227,705

between memories of unequal size, we will not sustain the Examiner's rejection of claim 81 under 35 U.S.C.

§ 103. The remaining claims on appeal also contain the above limitation discussed with regard to claim 81 and thereby, we will not sustain the rejection as to these claims under 35 U.S.C.

§ 103.

We have not sustained the rejection of claims 81 through 90 under 35 U.S.C. § 112 or under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

PATENT

ERROL A. KRASS)	
Administrative Patent Judge)	
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MICHAEL R. FLEMING)	BOARD OF
Administrative Patent Judge)	APPEALS AND
)	INTERFERENCES
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Appeal No. 96-2820
Application 08/227,705

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Appeal No. 96-2820
Application 08/227,705

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