The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 42

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TAKASHI HOSAKA

Appeal No. 1996-2702
Application No. 08/093,983

HEARD: MAY 9, 2001

Before THOMAS, RUGGIERO, and BARRY, Administrative Patent Judges.

RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal from the final rejection of claims 4-12. Claims 1-3 were canceled earlier in the prosecution of the application. Amendments after final rejection filed February 21, 1995, March 20, 1995, and May 1, 1995 were denied entry by the Examiner. A further amendment after final rejection filed May 30, 1995 concurrently with the filing of the Appeal Brief, which amended claims 4 and 10 and canceled claims 5, 8,

and 11, was approved for entry by the Examiner. Accordingly, only the rejection of claims 4, 6, 7, 9, 10, and 12 is before us on appeal.

The claimed invention relates to a method for forming a self-aligned contact in a MOS-type semiconductor device.

Claim 7 is illustrative of the invention and reads as follows:

> 7. A method of fabricating a MOS device, comprising the steps:
>
> forming a gate insulating film on a semiconductor substrate;
>
> forming a gate electrode film on the gate insulating film;
>
> forming a first insulating film on the gate electrode film;
>
> forming a first photoresist film on the first insulating film, the first photoresist film being patterned;
>
> patterning the gate electrode film and the first insulating film by using the first patterned photoresist film as a mask to form a patterned gate electrode film and first insulating film which are higher than the semiconductor substrate;
>
> forming low concentration impurity source and drain layers in a face of the semiconductor substrate by using the patterned gate electrode film as a mask;
>
> forming a second insulating film on an exposed surface of the gate insulating film and the first insulating film;

etching the second insulating film to form a side wall insulating film on the side wall of the gate electrode and to expose a surface of the semiconductor substrate;

forming high concentration impurity source and drain layers in a face of the semiconductor substrate by using the patterned gate electrode film and the side wall insulating film as a mask;

forming a conductor film on the exposed surface of the semiconductor substrate, the first insulating film and the side wall insulating film;

forming a second photoresist film over the conductor film;

patterning the second photoresist film by photolithography to form an opening over the gate electrode; and

etching the conductor film which is over the gate electrode in a desired shape, using the second patterned photoresist film as a mask.

The Examiner relies on the following prior art:

Taji	4,810,666	Mar. 07, 1989
Ku et al. (Ku)	5,010,039	Apr. 23, 1991 (filed May 15, 1989)
Favreau et al. (Favreau)	5,022,958	Jun. 11, 1991 (filed Jun. 27, 1990)
Kameyama et al. (Kameyama)	5,236,851	Aug. 17, 1993 (effectively filed Jul. 12, 1989)

Ghandhi, "Lithographic Processes," VLSI Fabrication Principles, pp. 534-38, 542-48 (1983).

Claims 4, 6, 7, 9, 10, and 12 stand finally rejected under 35 U.S.C. § 103. As evidence of obviousness, the Examiner offers Taji in view of Ghandhi and Kameyama with respect to claims 7 and

9, and adds Ku and Favreau to the basic combination with respect to claims 4, 6, 10, and 12.

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the Briefs[1] and Answer for the respective details.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the Examiner and the evidence of obviousness relied upon by the Examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellant's arguments set forth in the Briefs along with the Examiner's rationale in support of the rejection and arguments in rebuttal set forth in the Examiner's Answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would have suggested to one of ordinary skill in the art the invention as set forth in claims 4, 6, 7, 9, 10, and

[1]The Appeal Brief was filed May 30, 1995. In response to the Examiner's Answer dated August 31, 1995, a Reply Brief was filed November 6, 1995, which was acknowledged and entered by the Examiner without further comment as indicated in the communication of February 13, 1996.

12. Accordingly, we affirm.

As a general proposition in an appeal involving a rejection under 35 U.S.C. § 103, an Examiner is under a burden to make out a prima facie case of obviousness. If that burden is met, the burden of going forward then shifts to Appellant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1051-52, 189 USPQ 143, 147 (CCPA 1976).

With respect to independent claim 7, the Examiner, as the basis for the obviousness rejection, proposes to modify the MOS semiconductor device fabrication process disclosure of Taji. According to the Examiner, Taji teaches the claimed invention except that, while the patterning of a deposited metal layer for forming contacts 72, 74 is described (Taji, column 4, lines 4-9), there is no explicit disclosure of the use of photolithography in which a patterned photoresist is used as a mask to etch the deposited conductor film to a desired shape. To address this

deficiency, the Examiner turns to the photolithographic techniques disclosed by Ghandhi and Kameyama for etching conductor films. In the Examiner's view (Answer, pages 4 and 5), the skilled artisan would have been motivated and found it obvious to utilize photolithographic techniques as taught by Ghandhi and Kameyama for patterning the conductor film in Taji, thereby achieving precise patterning as well as protecting the device substrate during etching.

In our opinion, the Examiner's analysis is sufficiently reasonable that we find that the Examiner has at least satisfied the burden of presenting a prima facie case of obviousness. The burden is, therefore, upon Appellant to come forward with evidence or arguments which persuasively rebut the Examiner's prima facie case of obviousness. Only those arguments actually made by Appellant have been considered in this decision. Arguments which Appellant could have made but elected not to make in the Briefs have not been considered in this decision (note 37 CFR § 1.192).

In response, Appellant asserts the failure of the Examiner to establish a prima facie case of obviousness. According to Appellant (Brief, page 13; Reply Brief, page 8), the modification of Taji with Ghandhi and Kameyama would not result in the claimed

invention since none of the references disclose the claimed step of "patterning the second photoresist film by photolithography to form an opening over the gate electrode."

After careful review of the Taji, Gandhi, and Kameyama references in light of the arguments of record, we are in agreement with the Examiner's position as stated in the Answer. With regard to Taji, it is our view that, although Taji is silent about the manner of patterning the deposited metal layer to form contacts 72 and 74, the skilled artisan would appreciate that, in order to remove undesired portions of the metal layer to form the illustrated opening over gate 26 between contacts 72 and 74 (Taji, Figure 1h), the desired resultant contact portions must be protected from removal. We remain convinced that the skilled artisan, seeking guidance on implementing the metallization patterning operation in Taji would be led to the protective masking techniques in the photolithographic processes disclosed by Gandhi and Kameyama for all of the reasons articulated by the Examiner.

With regard to Ghandhi, while the Examiner has made particular reference to pages 547-48 which describe the process illustrated in Figure 7, we also find the description at pages 542-46 relating to the illustration in Figure 6 to be

particularly relevant. This illustrated technique involves a series of steps which form a window masking pattern in a photoresist film by photolithography. Similarly, we find that the teachings of Kameyama also provide a clear suggestion to the skilled artisan for the use of photolithographic protective masking techniques. In particular, the Figure 6c illustration and accompanying description in Kameyama disclose the use of a patterned photoresist layer 132A, 132B as a protective mask in the etching of conductive layer 114 to form an opening over a gate electrode. While Appellant is correct that Kameyama does not disclose the precise manner of patterning this photoresist layer, it is our view that the skilled artisan would appreciate that the use of photoresist layers is an integral part of applying photolithographic techniques for layer patterning.

As to Appellant's contention that Gandhi and Kameyama do not teach photolithographic patterning to form an opening over a gate electrode, we would point out that these references are used in <u>combination</u> with Taji to establish the basis for the obviousness rejection. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. <u>In re Keller</u>, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981); <u>In re Merck & Co.</u>, 800 F.2d 1091,

1097, 231 USPQ 375, 380 (Fed. Cir. 1986). The teaching for providing a conductive layer patterned to form an opening over a gate electrode already exists in the disclosure of Taji. In our view, the issue to be decided is the question of whether it would have been obvious to the skilled artisan to apply photolithographic techniques to formulate such patterned opening, which question we would answer in the affirmative based on our discussion supra. Further, although we find it sufficient that the skilled artisan was taught to use photolithographic techniques by Gandhi and Kameyama regardless of whether either of these references actually disclosed forming an opening over a gate electrode, we would point out that Kameyama clearly discloses in figures 6c and 6d the formation of an opening over a gate using a patterned photoresist.

For all of the above reasons, it is our opinion that, since the Examiner's prima facie case of obviousness has not been rebutted by any evidence or convincing arguments from Appellant, the Examiner's 35 U.S.C. § 103 rejection of independent claim 7, and dependent claim 9, the limitations of which have not been separately argued by Appellant, is sustained.

Turning to a consideration of the obviousness rejection of independent claims 4 and 10 based on the addition of Ku and

Favreau to the basic combination of Taji, Gandhi, and Kameyama, we sustain this rejection as well. Appellant contends (Brief, page 15; Reply Brief, pages 9 and 10) that even if the modified combination of Taji, Gandhi, and Kameyama were further modified to include the flattening films of Ku and Favreau, the resultant combination would not meet the claimed invention. In Appellant's view, neither of Ku nor Favreau disclose the etching back of a flattening film so that the thickness of the flattening film in regions over the gate electrode are thinner than other regions of the flattening film.

After reviewing the Ku and Favreau references in light of the arguments of record, our interpretation of these disclosures coincides with the Examiner's. Figures 1C-1G of Ku illustrate the thickness of flattening film 56 over the gate electrode 36 to be thinner than the thickness of the flattening film in adjacent regions on both sides of the gate electrode. Similarly, Figure 1 of Favreau illustrates that the thickness of flattening film 35 over the gate is thinner than regions adjacent to the gate.

Appellant's arguments suggest that Ku and Favreau have flattening film regions which are thicker over the gate electrodes than some other flattening film regions in contradistinction to the claimed invention. Although exactly

where this is the case has not been pointed out by Appellant, we would point out that, even assuming arguendo that this were the case, the present claim language requires only that the flattening film over the gate electrode be thinner than other flattening film regions, not all other flattening film regions as Appellant's arguments would have us interpret the claims.

Therefore, since Appellant's arguments have not overcome the Examiner's prima facie case of obviousness, the Examiner's 35 U.S.C. § 103 rejection of independent claims 4 and 10, and dependent claims 6 and 12 not separately argued by Appellant, is sustained.

In conclusion, we have sustained the Examiner's U.S.C. § 103 rejection of all of the claims on appeal. Accordingly, the decision of the Examiner rejecting claims 4, 6, 7, 9, 10, and 12 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

JAMES D. THOMAS Administrative Patent Judge	)	
JOSEPH F. RUGGIERO Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)	

JFR:hh

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