Paper No. 29

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte BRUNO FERRARIO

Appeal No. 96-2614
Application 08/098,740[1]

ON BRIEF

Before HAIRSTON, LEE and RUGGIERO, Administrative Patent Judges.

LEE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 1-22. No claim has been allowed.

References relied on by the Examiner

Pirez et al. (Pirez)	5,034,626	July 23, 1991
Carroll	5,130,571	July 14, 1992

[1] Application for patent filed July 28, 1993.

The applicant's admitted prior art as depicted in Figure 1 of the

specification.

The Rejections on Appeal

Claims 5 and 9 stand rejected under 35 U.S.C. § 103 as being unpatentable over the appellant's admitted prior art as depicted in Figure 1 of the specification, in view of Carroll.

Claims 1-3, 4, 6, 7, 8, 10, 11, 12-20, 21 and 22 stand rejected under 35 U.S.C. § 103 as being unpatentable over the appellant's admitted prior art as depicted in Figure 1 of the specification, in view of Carroll and Pirez.

The Invention

The invention is directed to a capacitance multiplier circuit (claims 1, 5 and 9), a method for providing a large RC time constant (claim 13), and a method for temperature compensating an RC circuit including a capacitor multiplier circuit (claim 17). Claims 1, 5, 9, 13 and 17 are the only independent claims. Claims 5 and 17 are representative and are reproduced below:

5. An integrated capacitance multiplier circuit comprising:

a capacitor having a first terminal connected to a lower common voltage, and also having a second terminal;

an operational amplifier having an output connected to an inverting input thereof, and having a non-inverting input connected to said second terminal of said capacitor;

a biasing circuit with at least two separate bias voltage outputs;

first and second field effect transistors having respective source regions thereof electrically connected together, and having respective gates connected to said bias voltage outputs of said biasing circuit;

said first transistor having a drain region connected to said second terminal of said capacitor, and

said second transistor having a drain region connected to said output of said operational amplifier; and

a multiplied-capacitance connection at said sources of said transistors; whereby said multiplied-capacitance connection provides an effective capacitance to said common voltage which is a multiple of the physical capacitance of said capacitor, multiplied in an amount which depends on the ratio of the conductances of said transistors.

17. A method for temperature compensating an integrated RC circuit which comprises an integrated resistor, an integrated capacitor and an integrated capacitance multiplier circuit capable of virtually multiplying the capacitance of said integrated

> capacitor by a term given by the ratio between two resistances to give a virtual capacitance value, comprising:
>
> (a) utilizing as said two resistances the ON resistances of two field effect transistors of different size;
>
> (b) biasing at least one of said transistors with a temperature dependent voltage for modifying the relative ON-resistance of the transistor and said ratio between ON resistances in function of temperature, thus varying said virtual capacitance value of the RC circuit in function of temperature to compensate a variation of the value of the integrated resistor of the RC circuit.

Opinion

The rejection of claims 1-22 cannot be sustained.

A reversal of the rejection on appeal should not be construed as an affirmative indication that the appellants' claims are patentable over prior art. We address only the positions and rationale as set forth by the examiner and on which the examiner's rejection of the claims on appeal is based.

In claims 1, 5 and 9, what is claimed is a capacitance multiplier circuit. In claim 13, what is claimed is a method for providing a large RC time constant. In claim 17, what is claimed is a method for temperature compensating an integrated

RC circuit. But in all of the appellant's claims, it is required that the resistance or conductance provided by two field effect transistors be used to enhance or multiply the capacitance otherwise provided by a capacitor. That is the key idea.

Capacitor multiplier circuits have been known. The appellant's Figure 1 illustrates the acknowledged prior art circuits of this kind. As is evident in a comparison of Figure 1 with appellant's claims, see for example claim 5, the prior art circuit makes use of two resistors R1 and R2, whereas the appellant's claims recite not first and second resistors but two field effect transistors with suitable biasing.

At page 4 of the answer, the examiner stated: "Note that although reference Carroll is used in this rejection to show that a transistor can be used as a resistor, the fact that a transistor can be used as a resistor is notoriously well known in the art . . . ." According to the examiner, "it is fundamentally basic and notoriously well known in the art that a transistor can function as a variable resistor by varying the biasing voltage, and that a transistor can function as a

constant resistor by biasing the transistor with a constant biasing voltage" (Examiner's Answer at page 10). The only evidence the examiner cited in support of the finding concerning using transistors as resistors is Carroll. The examiner stated (Answer at pages 8-9) that "Carroll teaches transistors can be used as resistors," that "[Carroll's] transistor operates as a switch but also as a resistor when it is turned on," and that "the resistance across the channel of the [Carroll] transistors is desirable and intentional."

We agree with the appellant that the examiner's reading of Carroll is misplaced and erroneous. The fact that transistors have intrinsic resistance/conductance does not translate or equate to a general teaching for using transistors as resistors. That such intrinsic resistance can be selected to vary the operating characteristics of a transistor in one way or another as a switch, either for changing the acquisition time or for affecting charge injection, is not a suggestion for using the transistor as a resistor. We have read the portions of Carroll cited by the examiner, i.e., column 1, lines 20-48, and column 2, line 67 to column 3, line 67, and do not find therein any teaching or

reasonable suggestion for using transistors as resistors. The transistors disclosed in Carroll are used only for switching purposes. While Carroll does discuss the equivalent resistance of a field effect transistor, it is only in the context of how it affects the charge time of a switched capacitor and switch induced charge injection. The examiner has not pointed to any portion of Carroll which reasonably would have suggested using a biased transistor not for its switching capabilities but as a resistor.

The examiner's important finding that it was notoriously well known in the art to use biased transistors as resistors is not supported by adequate factual evidence. Accordingly, the rejection of claims 5 and 9 over the admitted prior art and Carroll cannot be sustained.

The rejection of claims 1-4, 6-8, and 10-22 over the admitted prior art, Carroll, and Pirez also cannot be sustained because as applied by the examiner Pirez does not make up for the
above-discussed deficiencies of the admitted prior art and Carroll. The examiner has not articulated how Pirez would

have reasonably suggested using biased transistors as resistors.

While not necessary, we include the following discussion to indicate several points with which we disagree with the appellant. It may be useful if and when the examiner has found sufficient factual basis to support his finding that it was notoriously well known to use transistors as resistors. First, a transistor can be fixedly biased and thus a "biasing circuit" as recited in claim 1 can well be a power supply. Secondly, assuming that it would have been obvious to one with ordinary skill in the art to use a transistor as a resistor, it follows that any one or more resistor in a circuit may be implemented by a transistor, at the discretion of one with ordinary skill in the art. There is no reason to limit that discretion to an all or nothing choice. The motivation is simply the recognition that a

resistor may be implemented by a properly biased transistor and need not have anything to do with the appellant's focus on capacitance multiplier circuits.

We do not express a view one way or another with respect to the arguments of the appellant as directed to certain dependent claims, which we have not specifically addressed above.

Conclusion

The rejection of claims 5 and 9 under 35 U.S.C. § 103 as being unpatentable over the appellant's admitted prior art as depicted in Figure 1 of the specification, in view of Carroll. is reversed.

The rejection of claims 1-3, 4, 6, 7, 8, 10, 11, 12-20, 21 and 22 under 35 U.S.C. § 103 as being unpatentable over the

appellant's admitted prior art as depicted in Figure 1 of the specification, in view of Carroll and Pirez is reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)
JAMESON LEE Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
JOSEPH RUGGIERO Administrative Patent Judge	)

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