

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte WILLIAM J. KRUEGER  
and SRIRAM RAJAGOPALAN

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Appeal No. 1996-2481  
Application No. 07/828,763<sup>1</sup>

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ON BRIEF

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Before THOMAS, FLEMING, and BARRY, Administrative Patent Judges.  
BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the final rejection of claims 1-3, 11-21, and 42-45. The appellants filed amendments after final rejection on August 26, 1994 and October 30, 1995. Both were denied entry. We affirm-in-part.

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<sup>1</sup> The application was filed on January 29, 1992.

BACKGROUND

The invention at issue in this appeal relates to memory management. An erasable programmable read-only memory (EPROM) is erased by exposure to an ultraviolet light. In contrast, a flash-erasable programmable read-only memory (FEPRM), also called an electrically erasable programmable read-only memory (EEPROM), is erased by application of a certain voltage. A "block-erasable" FEPRM comprises blocks of memory that can be erased independently of each other. The invention provides memory management for allocating free space, deallocating allocated space, counting the number of erasures of a block, ensuring that each block has been erased about the same number of times, selecting a block in which to store data next, and reclaiming deallocated space for a block-erasable FEPRM.

Claim 1, which is representative for our purposes, follows:

1. A manager for a computer memory comprising:  
a block allocation routine, the memory divided  
into blocks of memory locations, each block having

an allocation table and a data region divided into data areas, each allocation table having entries corresponding to region data areas, the block allocation routine for selecting a block in which to store data;

a data area allocation routine for selecting a data area within the data region for the selected block in which to store data, for selecting an allocation table entry to correspond to the selected data area, and for setting the selected allocation table entry to correspond to the selected data area and to an allocated state; and

a storage routine for storing data in the selected data area.

The references relied on by the patent examiner in rejecting the claims follows:

Hoel et al. 1990 (Hoel)	4,942,541	Jul. 17,
Harari 1993. 6, 1990)	5,268,870	Dec. 7, (filed Aug.

Claims 1-3, 11-18, and 42-45 stand rejected under 35 U.S.C. § 102(b) as anticipated by Hoel. Claims 19-21 stand rejected under 35 U.S.C. § 103 as obvious over Harari. Rather than repeat the arguments of the appellants or examiner in toto, we refer the reader to the briefs and the answers for the respective details thereof.

OPINION

In reaching our decision in this appeal, we considered the subject matter on appeal and the rejections and evidence advanced by the examiner. We also considered the arguments of the appellants and examiner. After considering the record before us, we cannot say that the evidence anticipates the invention of claims 1-3, 11-15, and 42-45. It is our view, however, that it anticipates the invention of claims 16-18. In addition, it is our view that the evidence and level of skill in the art would have suggested the invention of claims 19 and 20. We cannot say, however, that these would have suggested the invention of claim 21. Accordingly, we affirm-in-part. Our opinion considers the anticipation of claims 1-3, 11-18, and 42-45 and the obviousness of claims 19-21 seriatim.

Anticipation of Claims 1-3, 11-18, and 42-45

We begin our consideration of claims 1-3, 11-18, and 42-45 by recalling that a prior art reference anticipates a claim only if it teaches expressly or inherently every limitation of the claim. Absence of any limitation from the

reference negates anticipation. Rowe v. Dror, 112 F.3d 473, 478, 42 USPQ2d 1550, 1553 (Fed. Cir. 1997). With this in mind, we address the appellants' arguments regarding claims 1-3, 13-15, and 42-45; regarding claims 11 and 12; and regarding claims 16-18 seriatim.

Claims 1-3, 13-15, and 42-45

Regarding claims 1-3 and 42-45 and relevant to claims 13-15, the appellants argue, "*Hoel's 'L-P map' is not equivalent to 'an allocation table.'*" (Appeal Br. at 11.) The examiner replies, "the allocation table of the claim and the L-P map serve the same purpose: to form a map between block/patch and data area." (Examiner's Answer at 5.)

We cannot find that Hoel teaches the allocation tables of the claims. Claims 1-3 and 42-44 specify in pertinent part a "memory divided into blocks of memory locations, each block having an allocation table ...." Similarly, claims 13-15 specify in pertinent part a "memory divided into blocks ... the method comprising the steps of: storing an allocation

table in each block, the allocation table having entries that indicate an offset of a data region within the block ...." Claim 45 likewise specifies in pertinent part a "memory being divided into blocks of memory locations, each block have a table ...." In short, the claims recite a separate allocation table for each of a plurality of memory blocks, i.e., a one-to-one relationship between allocation tables and memory blocks.

The examiner erred in not addressing the one-to-one relationship. Comparison of Hoel's disclosure to the claim language does not evidence that the reference teaches the claimed relationship. Hoel discloses an image processor and page printing system having a logical memory for mapping images and employing patchification. Col. 5, ll. 14-16. The system includes a processing unit 1 having a data bus 10, an address bus 11, and control lines 15. The processing unit has an address of 24 bits, viz., the address bits A(23, 22, ..., 1, 0), which represents an address space of 16 megabytes. The address bus includes a high order bit A(23), which connects on line 11-1 to control a multiplexor (MUX) 3. One

input to the MUX is the address bus 11-2 including the address bits A(22, 21, ..., 0). The address bus 11-3 includes the address bits A(15, 14, ..., 4), which are input to a permuter 2. The permuter transforms the address bits A(15, 14, ..., 4) and outputs the transformed address bits onto an output bus 12. Col. 13, ll. 15-31.

The MUX also receives the address bits A(20, ..., 16) and A(3, ..., 0), which are combined with the permuted address bits on the output bus. The address bits selected by the MUX and the A(23) address bit on line 11-1 are combined onto bus 13 as an input to a map unit 4. The map unit transforms a logical address input on bus 13 into a real address output on bus 14. The real address is the mapped address  $A_r$  (23, 22, ..., 0). Id. at ll. 31-40. Contrary to the claimed one-to-one relationship between allocation tables and memory blocks, the reference discloses only a single memory table, viz., map unit 4, for all memory blocks of the system. The absence of the claimed relationship from Hoel negates anticipation. Therefore, we reverse the rejection of claims 1-3, 13-15, and 42-45 under

35 U.S.C. § 102(b). Next, we address the appellants' arguments regarding claims 11 and 12.

Claims 11 and 12

Regarding claims 11 and 12, the appellants argue, "[i]n the Hoel system, the deallocation of physical patches does not involve copying data from one physical patch to another." (Appeal Br. at 15.) The examiner chose not to respond specifically to this argument. (Examiner's Answer at 12 ("no further discussion is required.").)

We cannot find that Hoel teaches the claimed copying. Claims 11 and 12 specify in pertinent part "copying allocated data regions from the block to be reclaimed to the spare block whereby a memory area corresponding to the deallocated data region is reclaimed for allocation." In short, the claims recite copying data from one memory block to an erased memory block.

The examiner erred in not addressing the copying. Comparison of Hoel's disclosure to the claim language does not

evidence that the reference teaches the limitation. The reference's system executes the following processes: painting, which creates and stores page image data; allocating, which maps logical addresses to physical addresses; shipping, which transmits the page image data to a printer; and deallocating, which returns physical patches to a queue after printing.

Col. 5, ll. 16-22.

More specifically, the deallocating process deallocates physical patches and returns the patches to an unordered queue. During shipping, the raster method of addressing a pure logical page image memory periodically causes all of the addresses within the boundary of a patch to have been accessed and the corresponding physical page image data to have been retrieved and printed. The contents of the physical patch that correspond to the target logical patch, after being printed, are restored to a condition by which the contents of the physical patch represent a blank page image. The physical patch has its reference to the corresponding logical patch removed from the map table and the location of the physical patch is returned to the

unordered queue of available physical patches. The logical patch is remapped to the common blank physical patch in preparation for creating a subsequent page. Col. 12, l. 63 - col. 13, l. 12.

The examiner fails to show that Hoel teaches copying data from one memory block to an erased memory block. The absence of the claimed copying negates anticipation. Therefore, we reverse the rejection of claims 11 and 12 under 35 U.S.C. § 102(b). Next, we address the appellants' arguments regarding claims 16-18.

#### Claims 16-18

Regarding claims 16-18, the appellants make two arguments. First, they argue, "the Hoel patent does not describe storing anything into a logical patch ...." (Appeal Br. at 17.) The argument refers to the claimed step of "storing a logical block number in each block ...." The rest of the appellants' specification does not indicate that their invention stores a logical number in a memory block. Storing a logical number in a memory block, moreover, appears self-defeating to the invention's "dereferencing of a handle,"

which is part of the invention. A handle includes a logical block sequence number, which indirectly references a region within a physical block of memory. The handle is dereferenced inter alia by determining the physical block that corresponds to the logical block sequence number. (Spec. at 13.) Storing a logical number in the physical block would obviate the need to translate the logical block number to a physical block number. Accordingly, the appellants' reliance on this limitation for patentability is not persuasive.

Second, the appellants argue, "the Hoel patent only describes one numbering system for logical patches ...." (Appeal Br. at 16.) The examiner responds, "[t]he basis of any map between logical and physical entities requires identification of the two entries which [sic] correspond. Hoel addresses this at a number of places ...." (Examiner's Answer at 8.)

We find that claims 16-18 do not define over Hoel. The claims specify in pertinent part the following limitations:

generating a mapping from each logical block number to the physical block number in which the logical block number is stored;  
receiving a logical block number; and  
translating the received logical block number to a physical block number using the generated mapping.

During patent examination, pending claims must be given their broadest reasonable interpretation. Limitations from the specification are not to be read into the claims. In re Van Geuns, 988 F.2d 1181, 1184, 26 USPQ2d 1057, 1059 (Fed. Cir. 1993); In re Prater, 415 F.2d 1393, 1404, 162 USPQ 541, 550 (CCPA 1969). Giving the claims their broadest reasonable interpretation, they recite translating a logical block number to a physical block number.

Hoel discloses that each logical patch has a unique identifying number which is extracted from the portion of the address output of the patchified logical page image memory, i.e., the patchified address. The subfield within the patchified address, viz., the patch identifier, is the portion of the output address which specifies a modulus of the common size of the linear physical patch within the system employing patchification. The patch identifier is input to a mapping table. The output of the mapping table is used to specify a

physical patch corresponding to a unique patch identifier.  
Col. 11, ll. 26-37.

The appellants erred in reading limitations from their specification into the claims. Comparison of Hoel's disclosure to the claim language evidences that the reference teaches the claimed translating of a logical block number to a physical block number. The unique identifying number or the patch identifier of the reference's logical patch teaches the claimed logical block number. Hoel's specifying of a physical patch corresponding to a unique patch identifier teaches the claimed translating to a physical block number. Therefore, we find that the reference teaches the limitations of claims 16-18. Next, we consider the obviousness of claims 19-21.

Obviousness of Claims 19-21

We begin our consideration of the obviousness of claims 19-21 by finding that the references represent the level of ordinary skill in the art. See In re GPAC Inc., 57 F.3d 1573, 1579, 35 USPQ2d 1116, 1121 (Fed. Cir. 1995) (finding that the Board of Patent Appeals and Interference did not err in

concluding that the level of ordinary skill in the art was best determined by the references of record); In re Oelrich, 579 F.2d 86, 91, 198 USPQ 210, 214 (CCPA 1978) ("[T]he PTO usually must evaluate ... the level of ordinary skill solely on the cold words of the literature."). Of course, every patent application and reference relies on the knowledge of persons skilled in the art to complement its disclosure. In re Bode, 550 F.2d 656, 660, 193 USPQ 12, 16 (CCPA 1977). Such persons must be presumed to know something about the art apart from what the references teach.

In re Jacoby, 309 F.2d 513, 516, 135 USPQ 317, 319 (CCPA 1962).

We also recall that in rejecting claims under 35 U.S.C. § 103, the patent examiner bears the initial burden of establishing a prima facie case of obviousness. A prima facie case is established when the teachings from the prior art would appear to have suggested the claimed subject matter to a person of ordinary skill in the art. If the examiner fails to establish a prima facie case, an obviousness rejection is improper and will be overturned. In re Rijckaert, 9 F.3d

1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). With this in mind, we analyze the appellants' arguments regarding claims 19, 20, and 21 seriatim.

#### Claim 19

As noted by the examiner, (Supplemental Examiner's Answer at 4), the appellants fail to address specifically the rejection of claim 19. They have shown no error in the rejection. Therefore, we affirm the rejection. Next, we address the appellants' arguments regarding claim 20.

#### Claim 20

Regarding claim 20, the appellants argue, "[t]here is nothing inherent in selecting storage that would require the selecting of multiple blocks, each with enough space to store the data." (Reply Br. at 3.) They add, "[t]he Harari patent also neither teaches nor suggests that an erase count should be used when identifying a block for allocation." (Id.) The examiner responds, "[o]n the contrary, a data set larger than available blocks is inherently stored in multiple blocks." (Supplemental Examiner's Answer at 4.) He adds, "[t]he

distinction between replacing a block at allocation, as opposed to erasure is specious. In both cases, there is a span of time between two actions on the block, erasure and allocation, and it is moot and arbitrary which end of the span is used." (Id.)

We find that claim 20 does not define over Harari. The claim specifies the following limitations:

A method of allocating a block in a block-erasable, programmable, read-only memory for the storage of data, the method comprising the steps of:  
maintaining an erase count for each block, the erase count indicating the number of times the block has been erased;  
selecting blocks with enough space to store the data; and  
identifying the selected block based on the erase count for the storage of data to effect the allocation of the block.

Giving the claim its broadest reasonable interpretation, it recites selecting a block to store data because the block has sufficient free space and based, in some way, on its erase count.

Harari relates to EPROMs and EEPROMs. Col. 1, ll. 13-16. The reference discloses an erasure algorithm that can be applied to any prior art Flash EEPROM. Col. 8, ll. 53-55.

The algorithm is based on the number of erasures experienced by each memory block, i.e., the erase count (S). Initially, the value of S is set at zero. It is incremented by one for each erase cycle. Each block stores its own value of S. When a block's value reaches a set number of erase cycles, the block can be replaced automatically with a new block. Col. 9, ll. 20-31.

The appellants erred in reading limitations from their specification into the claim. Comparison of Harari and the prior art as a whole to the claim language evidences that the reference would have suggested the claimed selecting of a block to store data because the block has sufficient free space and based, in some way, on its erase count. Even apart from what the reference discloses, a person skilled in the art seeking to store data in a memory block would have known to select only a block that has sufficient free space. Harari, moreover, discloses removing blocks with a certain erase count. Accordingly, only blocks with a lower erasure count can be selected. This suggests selecting of a block to store data based on its erase count. Therefore, we find that the

reference would have suggested the limitations of claim 20.

Next, we address the appellants' arguments regarding claim 21.

Claim 21

Regarding claim 21, the appellants argue, "[t]here is absolutely no teaching or suggestion in the Harari patent that data in blocks should be swapped to effect balancing of erase cycles." (Reply Br. at 4.) The examiner replies, "the rejection did not state that there was an explicit suggestion within Harari that blocks should be swapped." (Supplemental Examiner's Answer at 5.) He adds, "[t]he test is what Harari would suggest to one of ordinary skill in the art ...." (Id.)

We cannot find that Harari teaches or would have suggested the swapping of claim 21. The claim specifies in pertinent part following limitations:

identifying a first block that has been erased;  
identifying a second block that has been erased  
a fewer number of times than the first block; and  
swapping the data in the first block with the  
data in the second block.

In short, the claim recites swapping data of a block with data of another block that has been erased a fewer number of times to level erase counts.

As aforementioned, the examiner admits that Harari does not explicitly suggest the swapping. The examiner, furthermore, has not identified any suggestion in the prior art as a whole for the swapping. To the contrary, such swapping of data is counterintuitive. The number of erasure cycles that a EEPROM can endure is finite. Harari, col. 2, ll. 4-6. Because each block is erased as part of the claimed swapping process, which increases the erase count of each block, (Reply Br. at 4), it is not apparent that a person of ordinary skill in the art would have been motivated to perform the swapping. For the foregoing reasons, the examiner failed to show that Harari would have suggested the swapping of claim 21. Therefore, we find that the examiner's rejection does not amount to a prima facie case of obviousness. Because the examiner has not established a prima facie case, the rejection of claim 21 over Harari is improper. Therefore, we reverse the rejection of the claim under 35 U.S.C. § 103.

We end our opinion by concluding that we are not required to raise or consider any issues not argued by the appellants. Our reviewing court concluded, "[i]t is not the function of this court to examine the claims in greater detail than argued by an appellant, looking for nonobvious distinctions over the prior art." In re Baxter Travenol Labs., 952 F.2d 388, 391, 21 USPQ2d 1281, 1285 (Fed. Cir. 1991).

37 C.F.R. § 1.192(a), as amended at 60 Fed. Reg. 14518 (Mar. 17, 1995), was controlling when the appeal brief was filed. Section 1.192(a) stated as follows.

The brief ... must set forth the authorities and arguments on which the appellant will rely to maintain the appeal. Any arguments or authorities not included in the brief will be refused consideration by the Board of Patent Appeals and Interferences, unless good cause is shown.

Simultaneously, 37 C.F.R. § 1.192(c)(8)(iii) stated as follows.

For each rejection under 35 U.S.C. 102, the argument shall specify the errors in the rejection and why the rejected claims are patentable under 35 U.S.C. 102, including any specific limitations in the

rejected claims which are not described in the prior art relied upon in the rejection.

Also simultaneously, 37 C.F.R. § 1.192(c)(8)(iv) stated as follows.

For each rejection under 35 U.S.C. 103, the argument shall specify the errors in the rejection and, if appropriate, the specific limitations in the rejected claims which are not described in the prior art relied on in the rejection, and shall explain how such limitations render the claimed subject matter unobvious over the prior art. If the rejection is based upon a combination of references, the argument shall explain why the references, taken as a whole, do not suggest the claimed subject matter, and shall include, as may be appropriate, an explanation of why features disclosed in one reference may not properly be combined with features disclosed in another reference. A general argument that all the limitations are not described in a single reference does not satisfy the requirements of this paragraph.

In summary, section 1.192 provides that as the court is not under any burden to raise or consider issues not argued by the appellants, the Board of Patent Appeals and Interferences is also not under any such burden.

CONCLUSION

To summarize, the examiner's rejection of claims 1-3, 11-15, and 42-45 under 35 U.S.C. § 102(b) and of claim 21 under 35 U.S.C. § 103 is reversed. His rejection of claims 16-18 under § 102(b) and of claims 19 and 20 under 35 § 103 is affirmed.

No period for taking subsequent action concerning this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED-IN-PART

JAMES D. THOMAS	)	
Administrative Patent Judge	)	
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	)	BOARD OF PATENT
MICHAEL R. FLEMING	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
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LANCE LEONARD BARRY	)	
Administrative Patent Judge	)	

Appeal No. 1996-2481  
Application No. 07/828763

Page 23

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Appeal No. 1996-2481  
Application No. 07/828763

Page 24

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