THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 31

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JOHN W. PODUSKA, JR.

Appeal No. 96-2379
Application 07/837,240[1]

ON BRIEF

Before THOMAS, BARRETT and LEE, Administrative Patent Judges.

LEE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-20. No claim has been allowed. We affirm the rejection of claims 1-9 and 12-19 and reverse the rejection of claims 10, 11 and 20.

References relied on by the Examiner

Mori et al. (Mori)	5,294,984	Mar. 15, 1994 (filed Jan. 13, 1992)

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[1] Application for patent filed February 14, 1992.

Comins et al. (Comins)	5,179,641	Jan. 12, 1993 (filed Jun. 23, 1989)
Jarvis	3,961,134	Jun. 1, 1976

The Rejections on Appeal

Claims 1-6, 8, 10-18 and 20 stand finally rejected under 35 U.S.C. § 103 as being unpatentable over Comins.

Claim 7 stand finally rejected under 35 U.S.C. § 103 as being unpatentable over Comins and Mori.

Claims 9 and 19 stand finally rejected under 35 U.S.C. § 103 as being unpatentable over Comins and Jarvis.

The Invention

The invention is directed to a dithering technique for displaying an image that appears to have better resolution on a device that does not have enough color or intensity resolution to display an image of that quality. According to the appellant, the invention represents an improvement over prior art dithering techniques by not requiring a first comparing step which compares certain lower bits in the intensity information with pre-stored values before deciding whether the remaining upper bits of the intensity information are to be incremented.

Claims 1 and 3-12 are apparatus claims, and claims 2 and 13-

20 are process claims. Claims 1, 2 and 12 are independent claims, of which claims 1 and 2 are representative and are reproduced below:

1. An image processing device comprising:

an input register coupled to receive input data which includes location and intensity information of images to be displayed;

an interpolator register coupled to receive a dithering value which is dependent on the location information of the input data in the input register;

an adder coupled to said input register and said interpolator register and configured to provide a resultant value of the addition of the intensity information of the input data and the dithering value; and

an output register coupled to said adder for receiving a selected number of bits of the resultant value.

2. A method of generating an image including the steps of:

receiving input data including location information and intensity information;

adding a dithering value associated with the input data to the intensity information to generate a resultant value;

generating an output value including a selected number of bits of the resultant value; and

generating an image based upon said output value.

Claims 3-11 depend ultimately from claim 1, and claims 13-20

depend ultimately from claim 2.

Opinion

The rejection of claims 1-9 and 12-19

We sustain the rejection of claims 1-9 and 12-19.

This decision is based solely on the arguments raised by the appellants. We offer no opinion on arguments which could have been raised but which were not set forth in the appellant's brief.

The appellant's discussion of prior art dithering techniques, both in the specification and in the background section of the appeal brief, ignores the disclosure of Comins. According to the appellant, prior art dithering techniques require lots of processing steps and processing time by separating intensity data into integer and fractional bits, by comparing the fractional bits with a certain value in a dithering matrix, and then by incrementing the integer bits if the results of the comparison of fractional bits is within a certain range (Br. at 12-13). The appellant's invention eliminates the need to compare the fractional bits with the values in a dithering matrix, by adding the intensity information as a whole to a

dithering value to take advantage of the carry bit to accomplish any needed incrementation. This procedure saves processing time and circuitry as compared to prior art which requires a comparison operation for the fractional bits.

Like the appellant's claimed invention, Comins' technique eliminates the need to compare the fractional bits to values in a dithering matrix. In the argument portion of the appellant's brief at 16-17, the appellant acknowledges that in Comins, the least significant bits in the calculated pixel value are added to a dithering value in a first adder 264, and any carry bit is added to the more significant bits of the calculated pixel value in a second adder 265 (Figure 2). No comparison of the fractional or least significant bits of the input word or calculated pixel value with any stored value is required.

With respect to claims 1 and 12, it is true that Figure 2 of Comins does not disclose an interpolator register which "receives" a dithering value to be added to any portion of the calculated pixel value. Rather, a pseudo number PN generator 261 including a shift register is used to generate and output such a dithering value (Figure 2). We agree with the examiner, however, that registers are well known and are basic devices for storing and holding data (answer at 4-5), and thus it would have been

obvious to one with ordinary skill in the art to receive or buffer between digital circuit stages a generated dithering value in a holding or interpolator register prior to further processing. Alternatively, the shift register in the PN generator can be reasonably regarded as the claimed interpolator register, because it holds the dithering value before outputting the same to adder 264. We note that during patent examination, claim terms are properly interpreted according to their broadest reasonable interpretation consistent with the specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989); In re Yamamoto, 740 F.2d 1569, 1571, 222 USPQ 934, 936 (Fed. Cir. 1984); In re Pearson, 494 F.2d 1399, 1404, 181 USPQ 641, 645 (CCPA 1974); In re Prater, 415 F.2d 1393, 1404, 162 USPQ 541, 550 (CCPA 1969). Generating and holding is reasonably deemed one form of receiving. At a minimum, it reasonably suggests receiving.

Further with respect to claims 1 and 12, it is true that Figure 2 does not illustrate an output register coupled to the adder for receiving a selected number of bits of the resultant value. Instead, the second adder 265 directly provides the output. However, as the examiner correctly found, registers are well known and are basic devices for storing and holding data.

We agree with the examiner that it would have been obvious to one with ordinary skill in the art to first hold or buffer the resultant value in a register and then output the same. There is no reason why one with ordinary skill in the art would perceive that the resultant value must be provided directly from the adder and cannot first be placed in an output register. The basic skills of one with ordinary skill in the art would include such common sense and logical reasoning. Indeed, even the appellant's own specification describes and illustrates the use of output registers by prior art dithering techniques (Figure 3).

The appellant argues that while the claimed invention recites only a single adder, Comins makes use of two adders in sequence. The argument is misplaced. The rejection on appeal is one for obviousness, not anticipation. As is shown in Comins' Figure 2, the carry bit from the output of the first adder 264 is inputted to the second adder 265 which also take the more significant bits of the calculated pixel value as input. From the perspective of one with ordinary skill in the art, the two-adder structure of Comins is equivalent to a single larger adder. Logic dictates that adding the lower bits of a number to a value in a first adder and then feeding the carry data to a second adder which also takes as input the higher bits of the same

number is the same as adding the number in its entirety at once in a larger adder sufficient to add all of the bit positions. In our view, that is within the realm of the basic skills and common sense intrinsically possessed by one with ordinary skill in the art. It should be noted that a conclusion of obviousness may be made from common knowledge and common sense of the person of ordinary skill in the art without any specific hint or suggestion in a particular reference. In re Bozek, 416 F.2d 1385, 1390, 163 USPQ 545, 549 (CCPA 1969). That one number can be added to another in a single adder without splitting the first into two parts is not a novel idea by any means. Certain basic skills are to be presumed. See In re Sovish, 769 F.2d 738, 743, 226 USPQ 771, 775 (Fed. Cir. 1985) ("[The appellant's] argument presumes stupidity rather than skill"). We are not persuaded by the appellant that there is patentable distinction based on whether the carry bit is naturally carried in a single adder or externally carried through use of two adders.

In any event, neither the word “single” nor the words “natural carry” appear in any claim and we do not read the claims as requiring only a single adder or a “natural carry” operation.

With respect to all independent claims 1, 2 and 12, the appellant argues that the claimed invention requires input data

which includes both location and intensity information of the images to be displayed. In his answer, the examiner specifically points out and identifies, for the first time, where in Comins is disclosed such input data including both location and intensity information (answer at 7-8).

In the reply brief at 3 and 12-13, the appellant argues that prior to the examiner's answer, the examiner's position was that Comins did not disclose input data which includes both location and intensity information, and therefore it was unfair for the examiner to maintain an opposite position for the first time in the examiner's answer. The appellant asserts that at this late date it was too late to amend the claims and thus the examiner's taking a flip-flop is prejudicial to the appellant.

It does appear to us that the examiner has flip-flopped on his position with regard to the limitation at issue. However, that fact does not help the appellant in this appeal. If the appellant felt prejudiced by the examiner's action, the appropriate recourse would have been to petition the Commissioner for a re-opening of prosecution so that the new position of the examiner can be addressed or the claims amended. The appellant did not do that. Alternatively, the appellant can submit substantive arguments in the reply brief to rebut the new points

raised by the examiner. On this record, the examiner's position remains entirely unrebutted by the appellant as to how and why Comins discloses input words which include both location and intensity information. The appellant has not given us any reason to hold that the examiner's finding in that regard is erroneous.

For the foregoing reasons, we will sustain the rejection of independent claims 1, 2 and 12 under 35 U.S.C. § 103 as being unpatentable over Comins.

With regard to the further features added by dependent claims 5-9, 15, and 17-19, the appellant does not dispute the findings of the examiner and does not explain why the claimed subject matter would not have been obvious over the cited prior art except to note their dependence on an independent claim which is believed by the appellant to be allowable. Accordingly, these claims will fall with their corresponding independent claims.

With regard to claim 3 which recites that the adder comprises an adder circuit having a carry function, and claim 13 which recites that the adding step includes operating an adder circuit having an adder function, the issue is the same as that concerning an alleged distinction based on whether one or two adders are used for the adding function. In the appeal brief at 8, the appellant argues that the two adders of Comins are very

different and do not operate in the same manner as the single adder of the present invention. For reasons already discussed above in connection with independent claims 1, 2 and 12, we are not persuaded that the difference amounts to a patentable distinction. Alternatively, the claim language that the adder comprises an adder circuit having a carry function is so broad that it reads on an adder which sends the most significant carry bit to another adder. The fact that a carry bit exists satisfies the requirement that there is a carry function. Note that the broadest reasonable interpretation applies during patent examination.

With regard to claims 4 and 14, the appellant argues that in Comins the circuitry in workstation 10, which performs the addition functions, is not an arithmetic logic unit in a microcomputer. The argument is misplaced. In light of the digital logic disclosed by Comins for performing the adding function, it would have been obvious to one with ordinary skill in the art to implement the function through a digital microcomputer's arithmetic logic unit. The appellant nowhere explained why it would not have been obvious to one with ordinary skill in the art to use a microcomputer's arithmetic logic unit to implement an addition function. Note that 37 CFR

§ 1.192(c)(8)(iv) requires the appellant to explain why the issue at hand would render the claimed subject matter nonobvious to one with ordinary skill in the art. The appellant has not done that.

With regard to claim 16, which depends from claim 15, the appellant argues merely the distinctions based on features recited in claims 2 and 15. Accordingly, this claim will fall together with claims 2 and 15.

The rejection of claims 10-11 and 20

We do not sustain the rejection of claims 10-11 and 20.

Claim 10 depends from claim 1 and further recites that the dithering value is dependent on the location information of the next input data. Claim 11 depends from claim 1 and further recites that the dithering value is dependent on the location information of the input data and on the location information of the next input data. Claim 20 depends from claim 2 and recites that the step of adding a dithering value includes providing a dithering value which is dependent on the location information of the next input data. Thus, all of claims 10, 11 and 20 require that the dithering value is dependent on the location information of the next input data.

The examiner specifically acknowledges (answer at 5) that Comins does not disclose that the dithering value is dependent on

the location information of the next input data. However, based on the disclosure in Comins that the dithering value can be pseudo-random or randomly selected, the examiner concludes that it does not matter how the dithering value is chosen and therefore it would have been obvious to one with ordinary skill in the art to have a dithering value which is dependent on the location information of the next input data. We disagree.

The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992). Obviousness may not be established using hindsight or in view of the teachings of suggestions of the inventor. Para-Ordnance Mfg. v. SGS Importers Int'l, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995). A teaching of random selection does not equate to or reasonably suggests a dithering value which is specifically dependent on something in particular, in this case, the location information of the "next" input data. The examiner has not demonstrated that Comins discloses or would reasonably have suggested to one with ordinary skill in the art that it would be desirable to have the dithering value be dependent on the location information of the "next"

input word. Accordingly, the rejection is based on improper hindsight.

Conclusion

The rejection of claims 1-6, 8, and 12-18 under 35 U.S.C. § 103 as being unpatentable over Comins is affirmed.

The rejection of claim 7 under 35 U.S.C. § 103 as being unpatentable over Comins and Mori is affirmed.

The rejection of claims 9 and 19 under 35 U.S.C. § 103 as being unpatentable over Comins and Jarvis is affirmed.

The rejection of claims 10, 11 and 20 under 35 U.S.C. § 103 as being unpatentable over Comins is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

JAMES D. THOMAS Administrative Patent Judge	)	
LEE E. BARRETT Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND

	)	INTERFERENCES
	)	
	)	
JAMESON LEE	)	
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