

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte STEFAN P. SYWYK

Appeal No. 96-2091
Application No. 08/230,544¹

ON BRIEF

Before KRASS, MARTIN, and BARRETT, Administrative Patent Judges. KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1, 2 and 15 through 18², all of the claims pending in

¹Application for patent filed April 20, 1994. According to appellant, this application is a continuation of application 07/904,431 filed June 25, 1992, now U.S. Patent No. S,336,938 issued August 9, 1994.

²While the appendix to the principal brief indicates that claims 17 and 18 depend, respectively, from claims 4 and 5, they actually depend, respectively, from claims 16 and 17.

the application.

The invention is directed to apparatus for generating an asynchronous status flag with a predefined minimum active pulse length. The active pulse length of the status flag is the arbitrary length of time between a set signal and a clear signal. Where the delay between the set signal and the clear signal is below a predefined minimum pulse length time, the active pulse length of the status flag is defined by the predetermined minimum pulse length instead of the actual delay between the set signal and the clear signal.

Representative independent claim 1 is reproduced as follows:

1. An apparatus for generating a status flag comprising:

first input means for providing at least a first signal wherein said first signal activates said status flag;

second input means for providing at least a second signal wherein said second signal deactivates said status flag; and

circuit means for generating said status flag from the time delay between said first and second signals wherein said status flag has a predefined minimum active pulse length, said circuit means being coupled to receive said first signal from said first input means and being coupled to receive said second signal from said second input means.

The examiner relies on the following reference:

Appeal No. 96-2091
Application No. 08/230,544

Wong
1992

5,124,573

Jun. 23,

Appeal No. 96-2091
Application No. 08/230,544

Claims 1, 2 and 15 through 18 stand rejected under 35 U.S.C. 102(b) as anticipated by Wong.

Reference is made to the briefs and answer for the respective positions of appellant and the examiner.

OPINION

In accordance with appellant's grouping of the claims at page 3 of the principal brief, claims 1, 2 and 15 stand or fall, respectively, with claims 16, 17 and 18. Therefore, we will direct our attention to claims 1, 2 and 15.

At the outset, we note that the language of claim 1 appears, to us, to be a bit awkward. Referring to Figure 4, it would appear that the clear signal comes from a "first input means," that the set signal is from a "second input means" and that the circuit means for generating the status flag comprises elements 12, 13 and 14. Thus, we understand what the claim language intends to cover. However, while the

Appeal No. 96-2091
Application No. 08/230,544

claim is directed to apparatus for generating a status flag, the very first means provides a first signal which activates the status flag. It

appears odd to recite the activation of something which has not yet been generated. Similarly, the second means recites the deactivation of the status flag, the generation of which is the recited goal of the claimed subject matter. A circuit means then generates the status flag from the time delay between the first and second signals. However, the first and second signals activate/deactivate the very flag they are employed to generate in the first place.

In any event, since we understand the claimed subject matter sufficiently to apply prior art, we direct our attention to the rejection of the claims under 35 U.S.C. 102(b).

With regard to claim 1, we will sustain the rejection under 35 U.S.C. 102(b). Clearly, in Figure 1 of Wong, there

Appeal No. 96-2091
Application No. 08/230,544

is a "first input means" for providing at least a first signal (SET, on line 18) for activating a signal (CLOCK OUT); a "second input means" for providing at least a second signal (RESET on line 30) which deactivates the signal (CLOCK OUT) and a "circuit means" for generating the signal from a time delay between the first and second signals.

Appellant first argues that Wong, being directed to a clock chopper/expander, does not generate a "status flag" which is "both functionally and structurally distinguishable from the clock chopper/expander" [principal brief, page 3]. We are unpersuaded by this argument. The CLOCK OUT signal of Wong is a signal derived from first and second signals in the manner set forth in instant claim 1 and we find no functional or structural difference between this signal and the claimed "status flag," any difference being simply one of the label attributed thereto.

Appellant also argues [principal brief, page 4] that Wong does not disclose an apparatus which has a circuit means for generating a status flag from the time delay between the first

Appeal No. 96-2091
Application No. 08/230,544

and second signal wherein the first signal activates the status flag and the second signal deactivates the status flag. We disagree. The SET signal of Wong clearly "activates" the CLOCK OUT signal and the RESET signal of Wong clearly "deactivates" the CLOCK OUT signal. Further, the CLOCK OUT signal is generated from a time delay between the SET and RESET signals. Since the SET signal is activated by the CLOCK IN signal and the CLOCK IN signal is then delayed by element 22 with the delayed signal being employed to generate the RESET signal, quite clearly the

CLOCK OUT signal (i.e., the "status flag") is generated from a time delay between the first and second signals, as claimed.

Appellant further argues [principal brief, page 4] that Wong does not disclose that the status flag has a predefined minimum active pulse length and suggests, on the contrary, that a very narrow CLOCK IN transition will show at the output, referring to column 4, lines 48-55 of Wong. Again, we

Appeal No. 96-2091
Application No. 08/230,544

disagree with appellant.

Whatever the width of the CLOCK IN transition, Wong provides for a CLOCK OUT signal (which is the claimed status flag) having a stable pulse width. See Figures 2A and 2B of Wong. Since the pulse width is stable, or substantially constant, it is clear that this width is a "predefined minimum active pulse length" (albeit also a maximum active pulse length), as claimed. Accordingly, while we recognize the difference between the instant disclosed invention and that of Wong, in our view, a reasonable interpretation of the instant claim language permits the "predefined minimum active pulse length" to read on the constant pulse width of Wong's CLOCK OUT, or status flag, signal.

Thus, we will sustain the rejection of claim 1 (and claim 16) under 35 U.S.C. 102(b) as anticipated by Wong.

We reach a different conclusion with regard to instant claim 2. Claim 2 requires that the first and second signals

Appeal No. 96-2091
Application No. 08/230,544

be "asynchronous." The examiner contends that the SET signal of Wong, derived from the CLOCK IN signal, is "asynchronous" with the RESET signal, derived from a delayed version of the CLOCK IN signal, since the SET and RESET signals are "not aligned in phase" [supplemental answer, page 2]. The examiner also contends that since the TEST and CLOCK IN signals are "asynchronous" and are used to generate the first and second signals, the first and second signals must also be "asynchronous."

Appellant has defined "asynchronous" as "having no predetermined or fixed time relationship to one another" [specification, top of page 3]. In Wong, since the SET and RESET signals are both derived from the CLOCK IN signal, the SET and RESET signals cannot be "asynchronous," as that term is employed in the instant claims. With regard to the examiner's CLOCK IN/TEST signal explanation, these signals are applied alternatively. If there is a TEST signal (HIGH) and no CLOCK IN

signal (LOW), then the TEST signal passes through gate 14 as

Appeal No. 96-2091
Application No. 08/230,544

the SET signal and the RESET signal on line 30 is related to the TEST signal since it is derived from the CLOCK OUT signal which was derived from the TEST signal. If the TEST signal is low and the CLOCK IN signal is high, then both the SET and RESET signals are derived from the CLOCK IN signal, and, again, they are not "asynchronous," as that term is employed in the instant claims.

Accordingly, since Wong does not disclose the "asynchronous" first and second signals of instant claim 2, the subject matter of claim 2 is not anticipated by Wong under 35 U.S.C. 102(b). Claim 17 stands with claim 2.

Since claim 2 is not anticipated by Wong, neither can claim 15, dependent on claim 2, be anticipated by Wong under 35 U.S.C. 102(b). Claim 18 stands with claim 15.

We have sustained the rejection of claims 1 and 16 under 35 U.S.C. 102(b) but we have not sustained the rejection of claims 2, 15, 17 and 18 under 35 U.S.C. 102(b).

Appeal No. 96-2091
Application No. 08/230,544

Accordingly, the examiner's decision is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR 1.136(a).

AFFIRMED-IN-PART

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ERROL A. KRASS))
Administrative Patent Judge)	
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)	BOARD OF PATENT
JOHN C. MARTIN))
Administrative Patent Judge)	APPEALS AND
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LEE E. BARRETT))
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EAK/jlb

Appeal No. 96-2091
Application No. 08/230,544

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