

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RAMAN K. SUD, CHRIS KOVERMAN,
JINGSONG CAI and THOMAS HILL

Appeal No. 96-1979
Application 08/041,770¹

ON BRIEF

Before KRASS, TORCZON and CARMICHAEL, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1, 3 through 13 and 15 through 24, all of the claims remaining in the application.

¹ Application for patent filed April 02, 1993.

The invention is directed to an apparatus and method for fault tolerant operation of a multiprocessor data processing system. More particularly, the invention concerns the identification of a failed master processor and the subsequent designation of a new master processor for the failed master processor. The identification is said to be performed in a “dynamic” manner wherein a contention operation is utilized such that each processor contends with other processors to become the new master processor by writing its tag on all of the processors in the system. Once a processor has tagged each of the operating processors, it declares itself the new master by, for example, writing a master identification tag on each processor. Only a single new master processor will be declared.

Independent apparatus claim 1 is reproduced as follows:

1. A fault tolerant multiple processor data processing system, comprising:

a plurality of processors including a master processor which coordinates the operation of said plurality of processors;

means for connecting said plurality of processors to form a local area network;

a plurality of memory devices coupled to said plurality of processors;

means for identifying a failure of said master processor; and

means for assigning a new master processor from said plurality of processors, in a dynamic manner, after said failure of said master processor, said assigning means including means for executing a contention operation wherein each processor of said plurality of processors contends to become said new master processor by attempting to write a tag on each processor of said plurality of processors.

The examiner relies on the following references:

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Stiffler et al.	4,608,631	Aug. 26, 1986
Ely et al.	5,003,464	Mar. 26, 1991

Claims 1, 3 through 13 and 15 through 24 stand rejected under 35 U.S.C. 103. As evidence of obviousness, the examiner cites Ely with regard to claims 1 and 13, adding Stiffler with regard to the dependent claims 3 through 12 and 15 through 24.

Reference is made to the briefs and answer for the respective positions of appellants and the examiner.

OPINION

We reverse.

Turning to the rejection of the independent claims 1 and 13 under 35 U.S.C. 103 as unpatentable over Ely, the examiner recognizes that Ely fails to disclose the writing of a tag to each processor but takes Official notice that writing data to multiple stores of a multi-processor system to maintain data consistency is well known and concludes that it would have been obvious to modify Ely “with a means of distributing the status information stored in a single register to multi-storage devices of each processors [sic]” [final rejection - page 3], the motivation being to “enhance the reliability and fault tolerance of the multi-processing system” [final rejection - page 4].

The motivation ascribed by the examiner to the skilled artisan appears to have resulted from

impermissible hindsight. We find no reason for the artisan to have modified Ely in the manner described by the examiner.

While we can agree, in general, that it was well known to write data to multiple stores of a multi-processor system in order to maintain data consistency, it would appear that such was well known in cache environments so that each processor has access to the same data in memory but we agree with appellants [reply brief - page 2] that “the concept of cache tags has no nexus to the present invention.” Clearly, such cache tags are employed for data consistency and have no relationship to the contention operation during a system failure of the instant claimed invention. Thus, the examiner’s reasoning for modifying Ely to provide for the claimed tag writing to each processor is faulty and no prima facie case of obviousness is seen to have been established.

We further agree with appellants that Ely appears to “teach away” from the claimed subject matter because, whereas the instant claimed subject matter involves the exchange of messages between each processor, Ely explicitly avoids such a system as being too “slow, tedious and expensive, particularly in attempting to handle pluralities of simultaneous failures” [Ely, column 4, lines 7-10]. Accordingly, the artisan would hardly look to the disclosure of Ely, which teaches the selection of a replacement master processor by setting the order of selection by preselecting the order in which the requests by processors to take over the function of master processor are queued [Ely, column 5, lines 7-15], as a suggestion to provide an assigning means for executing a contention operation wherein each

processor contends to become the new master processor by attempting to write a tag on each processor of the plurality of processors.

Even though not applied against independent claims 1 and 13, we consider Stiffler since it was applied in combination with Ely with regard to the dependent claims. However, we do not find anything within the disclosure of Stiffler which would provide for the deficiencies noted supra with regard to Ely. Thus, while Stiffler does provide for a processor writing a tag to itself in a contention operation in attempting to become the master processor [bottom of column 10 to the top of column 11], we find nothing in Stiffler, and the examiner has not convincingly identified anything in Stiffler, which would suggest each of the processors attempting to write a tag on “each processor of said plurality of processors,” in a contention operation, as required by independent claims 1 and 13.

Accordingly, the examiner’s decision rejecting claims 1, 3 through 13 and 15 through 24 under 35 U.S.C. 103 is reversed.

REVERSED

ERROL A. KRASS)
Administrative Patent Judge)
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) BOARD OF PATENT

Appeal No. 96-1979
Application 08/041,770

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