

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MASAYUKI KOIZUMI and HARUYUKI MIYATA

Appeal No. 96-1844
Application No. 08/125,396¹

HEARD: May 06, 1999

Before THOMAS, KRASS, and GROSS, Administrative Patent Judges.

GROSS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1 through 33, which are all of the claims pending in this application.

Appellants' invention relates to a semiconductor device with analog and digital circuits formed in one semiconductor substrate. Claims 1 and 16 are illustrative of the claimed

¹ Application for patent filed September 23, 1993.

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invention and appear in the appendix to Appellants' brief, on pages 17 and 26, respectively.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Jarrett	4,595,909	Jun. 17, 1986
Fujita et al. (Fujita)	JP 4-251970 ²	Sep. 08, 1992

Claims 1 through 33 stand rejected under 35 U.S.C. § 103 as being unpatentable over Fujita in view of Jarrett.

Reference is made to the Examiner's Answer (Paper No. 11, mailed December 6, 1995) for the examiner's complete reasoning in support of the rejections, and to Appellants' Brief (Paper No. 10, filed October 30, 1995) for Appellants' arguments thereagainst.

OPINION

We have carefully considered the claims, the applied prior art references, and the respective positions articulated by Appellants and the examiner. As a consequence of our review, we will reverse the obviousness rejection of claims 1 through 33.

² Our understanding of this reference is based upon a translation provided by the Scientific and Technical Information Center of the Patent and Trademark Office. A copy of the translation is enclosed with this decision.

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Claims 1 through 15 and 21 through 26 all require "a first protection element . . . and a second protection element formed in said semiconductor body." Claims 19, 20, and 29 through 33 include the same limitation, but with the phrase "protecting element" in 19 and 20 and "protection circuit element" in 29

through 33 instead of "protection element." The examiner asserts

(Answer, page 3) that "Fujita teaches the entire structure of Appellant's [sic] claimed semiconductor device excluding portions drawn to separate power supplies for different wells." In other words, the examiner contends that Fujita includes first and second protection elements. Appellants respond (Brief, page 13) that "the combination of Fujita and Jarrett does not teach or suggest a first protection element and a second protection element" and that "[b]oth Fujita and Jarrett are totally silent concerning these features." We find no such elements in Fujita nor in Jarrett. Furthermore,

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the examiner not only has provided no guidance as to where he believes the elements are in the references, but also has failed to respond to appellants' arguments concerning the lack of protection elements. Accordingly, we cannot sustain the rejection of claims 1 through 15, 19 through 26, and 29 through 33.

Claims 1 through 15 and 21 through 26 further recite "fifth bias means for biasing said semiconductor body . . . said fifth bias means being independent from at least said third bias means," where the third bias means biases the inner well region of the digital circuit. Claims 27 through 33 similarly recite a

fifth bias means, but which is "different from said third bias means." Claims 16 through 20 require a "bias means for applying a potential to said semiconductor body, said bias potential being derived from a power source different from said second power source means," where the second power source means

supplies an operating power source voltage to the digital circuit.

In Figures 1 and 2 of Fujita, the substrate (10) (or semiconductor body) and the inner well (16) of the digital circuit region are connected to the same low potential power supply wiring (42 in Figure 1, 42A in Figure 2). (See also Fujita translation, page 7, lines 10-13 and page 8, line 26-page 9, line 2). In Figure 3, substrate (10) is connected to VCC2 by power supply line (42B) which biases inner well (16) of the digital circuit region. (See also Fujita translation, page 9, line 25-page 10, line 9). Accordingly, in all embodiments, the semiconductor body bias means is neither independent nor different from the bias means for the third well nor derived from a power source different from that of the digital circuit.

The examiner states (Answer, page 3) that Fujita does not teach separate power supplies for different wells. The examiner turns to Jarrett, asserting that "Jarrett teaches applications for ADC's and DAC's wherein . . . particularly in column 5 lines

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12-17 separate power supply terminals are taught 'which ensures that any changes in load currents during switching do not cause spiking at power supply terminal.'" The examiner concludes that "[i]t would have been obvious to a skilled artisan to apply the teachings of Jarrett to provide separate power terminals in the device of Fujita in order to avoid power spikes as taught by Jarrett."

Jarrett does suggest that using separate power supply terminals avoids spiking. However, Jarrett says nothing about supplying a semiconductor substrate with a separate power supply. Further, Fujita already includes multiple power supply lines to reduce noise passing through the power supply line. Therefore, without some specific teaching to use a separate bias means for the semiconductor substrate, one of ordinary skill in the art would not have been motivated to add yet another power supply terminal for the semiconductor substrate in the device of Fujita. Consequently, the broad suggestion of Jarrett to use separate power supply terminals is insufficient to establish a prima facie case of obviousness in this case.

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CONCLUSION

The decision of the examiner to reject claims 1 through
33 under 35 U.S.C. § 103 is reversed.

REVERSED

JAMES D. THOMAS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
ERROL A. KRASS)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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