

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 31

MAILED

UNITED STATES PATENT AND TRADEMARK OFFICE

OCT 17 1996

PAT.&T.M. OFFICE  
BOARD OF PATENT APPEALS  
AND INTERFERENCES

BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

Ex parte JEN-HSUN HUANG, MICHAEL D. ROSTOKER  
and DAVID GLUSS

Appeal No. 96-1728  
Application 07/937,643<sup>1</sup>

ON BRIEF

Before THOMAS, KRASS and JERRY SMITH, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 12 through 21, all of the claims remaining in the application.

<sup>1</sup> Application for patent filed August 31, 1992. According to Appellants, this application is a continuation in part of Application 07/911,846 filed July 10, 1992, now Patent No. 5,339,262 issued August 16, 1994.

The invention pertains to a method of emulating an electronic system for functional testing and is described in independent claim 12 reproduced as follows:

12. A method of emulating an electronic system for functional testing;

the electronic system including a support member, a system device formed on the support member, a first connector that is formed on the support member and operatively connected to the system device, and a core-cell based Application Specific Integrated Circuit (ASIC) that interconnects with the first connector;

the ASIC comprising a core-cell, and electronic core devices that are operatively connected to the core-cell;

the method comprising the steps of:

(a) constructing and operatively interconnecting the support member, system device and first connector;

(b) constructing a test pod to include a Field-Programmable Circuit Board (FPCB), a Field-Programmable Interconnect (FPIC) that is mounted on the FPCB, a core unit that is mounted on the FPCB and is substantially functionally equivalent to the core-cell, programmable logic devices that are mounted on the FPCB, and a second connector that is mounted on the FPCB and interconnects with the first connector;

(c) programming the FPIC to operatively interconnect the core unit, logic devices, and second connector via the FPCB; and programming the logic devices such that they are substantially functionally equivalent to core devices; such that the test pod is substantially functionally equivalent to the ASIC;

(d) interconnecting the first and second connectors such that the support member, system device and test pod emulate the electronic system; and

(e) functionally testing the support member, system device and test pod.

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The examiner relies on the following reference:

Sample et al. (Sample) 5,109,353 April 28, 1992  
(filed Dec. 2, 1988)

Claims 12 through 21 stand rejected under 35 U.S.C. 102(e) as anticipated by Sample. Additionally, claims 12 through 21 stand provisionally rejected under the judicially created obviousness-type double patenting over claims 12 through 39 of Application Serial No. 08/335,092 in view of appellants' admitted prior art.

Reference is made to the brief and answer for the respective details of the positions of appellants and the examiner.

#### OPINION

Turning first to the rejection of claims 12 through 21 under obviousness-type double patenting, appellants do not argue the rejection on its merits but, rather, request "that action on the double patenting issue be deferred until one or the other of the applications issues as a patent" [page 5, brief]. The examiner accedes to this request by agreeing "that action on this rejection should be deferred until the issuance of one of the applications as a patent" [page 6, answer]. Thus, we understand that the obviousness-type double patenting rejection is no longer being raised at this time and, accordingly, we will treat the rejection as being withdrawn by the examiner and we make no

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decision on the merits regarding the obviousness-type double patenting rejection.

We now turn to the rejection of claims 12 through 21 under 35 U.S.C. 102(e).

Anticipation, under 35 U.S.C. § 102, requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983).

In spite of the examiner's "unshakable position" [page 2, advisory action of August 7, 1995], we do not find the presence, in Sample, of a FPCB and a FPIC, a core unit functionally equivalent to a core-cell, and programmable logic devices, mounted on that FPCB, as set forth in step (b) of instant claim 12. Further, without a clear teaching of these claimed elements by Sample, the reference cannot provide for step (c) of instant claim 12 which requires "programming the FPIC to operatively interconnect the core unit, logic devices, and second connector via the FPCB; and programming the logic devices such that they are substantially functionally equivalent to core devices..."

In the rationale supporting the rejection, at pages 4-5 of the answer, the examiner sets forth a reasonable statement regarding the teachings of Sample. However, the examiner never

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sets forth any explanation as to the correspondence of Sample's teachings to the elements and steps of the instant claimed invention. It would be very helpful, to the Board, to applicants and to the examiner himself/herself, if the examiner would point out the correspondence, by identifying particular elements in the reference(s), between claimed elements/steps and those disclosed by the applied reference(s) when applying a rejection over prior art.

Since Sample never mentions anything about FPCBs, FPICs, core units and core-cells, and it is not at all clear how these claimed elements are being read on the reference, it was the examiner's burden to particularly point out what is being relied on in Sample for the teaching of these elements and their claimed interconnection.

In response to appellants' arguments regarding the lack of teaching by Sample of steps (b) and (c) of instant claim 12, the examiner merely cites portions of Sample at column 5, lines 26-30, column 6, lines 9-13, column 1, lines 52-64, column 11, line 5 to column 12, line 11, column 3, line 59 to column 4, line 8 and column 5, lines 26-43 [pages 7-9, answer] and concludes therefrom that

This clearly teaches the test pod and core unit which the applicant's [sic, applicants] state in the response that Sample et al. does not show [page 9, answer].

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Our perusal of the entire disclosure of Sample and of the portions cited by the examiner, in particular, indicates no mention of a test pod and core unit. Therefore, it remains unclear to us how the examiner arrives at such a "clear teaching" of a test pod and core unit by Sample. If there is something in Sample which the examiner regards as equivalent to these claimed elements, the examiner should explicitly identify those disclosed elements in Sample.

Since the examiner has failed to establish a prima facie case of anticipation of independent claim 12, there can be no anticipation of dependent claims 13 through 21 based on the applied reference.

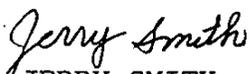
The examiner's decision rejecting claims 12 through 21 under 35 U.S.C. 102(e) is reversed.

REVERSED

  
JAMES D. THOMAS )  
Administrative Patent Judge )

  
ERROL A. KRASS )  
Administrative Patent Judge )

) BOARD OF PATENT  
) APPEALS AND  
) INTERFERENCES

  
JERRY SMITH )  
Administrative Patent Judge )

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