

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 27

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte KEVIN R. GRIESS,  
ANN C. MERENDA and  
DONALD L. PIERCE

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Appeal No. 96-1439  
Application 08/338,976<sup>1</sup>

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ON BRIEF

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Before THOMAS, JERRY SMITH and FLEMING, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

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<sup>1</sup> Application for patent filed November 14, 1994. According to the appellants, this application is a continuation of Application 07/807,696, filed December 16, 1991.

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DECISION ON APPEAL

Appellants have appealed to the Board from the examiner's final rejection of claims 1 to 20, which constitute all the claims in the application.

Representative claim 11 is reproduced below:

11. A method for dynamically handling processing errors in a computer system having a plurality of functional units, comprising the steps of:

detecting an error occurring during processing of an operation by a functional unit;

determining that said error was caused by a timing dependent defect; and,

after said determining step causing said functional unit to process subsequent operations in a degraded performance mode such that said error will not recur.

The following reference is relied on by the examiner:

Missios et al. (Missios)	4,025,768	May 24,
1977		

Claims 1 to 20 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon Missios alone.

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Rather than repeat the positions of the appellants and the examiner, reference is made to the briefs and the answer for the respective details thereof.<sup>2</sup>

#### OPINION

We sustain the rejection of claims 1, 5, 6, 11 to 13, 15, 17 and 18 but reverse the rejection of the remaining claims, comprising claims 2 through 4, 7 through 10, 14, 16, 19 and 20.

At the outset, we note our reliance in *Missios* upon Fig. 1, the abstract, the summary of the invention as well as the discussion beginning at col. 2 with respect to Fig. 1 through at least the top of col. 4 also further relating to that figure. The discussion in the initial paragraphs at col. 2 as to Fig. 1 relates to the notion of showing in Fig. 1 a program flow and particular predetermined "operation or associated group of operations" performed by the representative exemplary

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<sup>2</sup> On June 5, 1996, appellants filed a paper notifying the Board of a related appeal as to Application Serial No. 08/480,106, filed on June 7, 1995, which has been assigned Appeal No. 97-0609.

system in Fig. 2. This analogizes to a sequence of programming operations by program instruction sequencing, which is further buttressed by the statement at col. 4, beginning at line 36 relating to the operation of a program counter utilized to control the sequencing of "operations so as to provide a desired program flow." Column 4, lines 43 and 44.

Notwithstanding appellants' and the examiner's respective positions in the briefs and answer, it appears to us that the claimed first means corresponds to the operations performed at step D3 in Fig. 1 while the operations performed in claim 1's second means corresponds to the function in program flow position D6. This first recitation of a retry operation in claim 1 does not require it to be performed at the same or a different (higher or lower) clock cycle time. Continuing, the claimed third means also relates to the node exiting the D6 program flow block in Fig. 1 while the claimed fourth means relates to the operations performed at labeled block D9. The "varying" instruction processing cycle time of the claim does not indicate whether it is increased or decreased. The discussion at col. 2 of Missios indicates that the same

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predetermined clock signals or program "operations" are performed at the respective block labels D. Thus, to the extent claimed there is clear recitation of a plurality of retry operations even though it appears that previously executed operations are again performed in their entirety for the entire sequence of operations for each node position or block D. The claim does not exclude such an understanding of the claim. Again, as to the claimed varying operation of the processing cycle time, the reference in its entirety makes clear that the testing operations are performed at reduced clock frequencies.

We reverse the rejection of dependent claim 2 because there is no teaching or suggestion in Missios or persuasive line of reasoning advanced by the examiner for the requirement of this

claim for initiating a deferred service call under the conditions specified in the claims. Furthermore, because claims 3 and 4 depend in turn from claim 2, the rejection of claims 3 and 4 is also reversed.

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Turning next to independent claim 5 on appeal, we sustain the rejection here essentially for the same reasons as we did for claim 1 on appeal. The additional requirement that the error is caused by a timing dependent defect is clearly taught by the reference since it is stated to be a feature of the reference at least in the second sentence of the abstract. A feature of dependent claim 6 on appeal has already been discussed with respect to our earlier views as they apply to our affirmance of the rejection of claim 1.

We reverse the rejection of claim 7 because the feature of iteratively increasing the instruction processing cycle time does not appear to be taught or suggested in the reference until the first of two alternative conditions may have occurred. The examiner's position in the answer does not detail a discussion of this claim. The rejection of claim 8 is reversed for the same reason as we reversed the rejection of claim 2 as to the deferred service call recitation. Since claims 9 and 10 depend from claim 8, the rejection of them is reversed as well.

Turning next to the rejection of claim 11, we sustain this rejection. It contains a similar feature of the timing

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dependent defect as independent claim 5 on appeal. However, we note that there is no recitation of any retry let alone a plurality of retry operations in this claim. Therefore, the subject matter of this claim is more easily met by the above-noted teachings of the reference as we outlined earlier. Contrary to appellants' apparent assertions in the brief, we do not construe the degraded performance mode of operations to require an interpretation that any fault tolerance or error recovery is necessarily mandated by that language. This view is consistent with our affirmance of the feature recited in claim 12 because all that recited feature of degradation of performance in claim 11 means is simply that it is performed at a reduced clock speed, which feature we have clearly indicated before is contained within Missios.

We sustain the rejection of claim 12 further in view of the admitted prior art by appellants in the paragraph bridging pages 2 and 3 of the disclosed invention as it relates to redundant processing elements. It clearly would have been obvious to the artisan to have applied the teachings of Missios to a system embodying more than one "processing element." The rejection of dependent claim 13 is sustained

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for the same but amplified reasons since the feature of continuing the processing of a remainder of functional units when one has been determined to have an error is met by the capability expressed in the paragraph bridging pages 2 and 3 of the disclosure as to features known in the art. When one processing element is determined to have an error in the prior art, the remaining processing elements are continued or allowed to continue processing a stream of instructions while the one with the error is taken "off-line." Because the remaining active elements are stated to continue processing the instruction stream, the same performance level appears to have been met by the prior art approach as set forth in the last lines of claim 13 on appeal.

We reverse the rejection of dependent claim 14 because neither Missios nor appellants' admitted prior art indicates that the degraded mode comprises the feature of operating the one functional unit at a reduced clock speed while continuing to operate the others at a normal clock speed.

Finally, we turn to the features in independent claim 15 on appeal. Again, the rejection of this claim is sustained for the reasons set forth earlier. The rejection of claim 16

is reversed for the same reasons we reversed the rejection of claim 2. The features recited in dependent claims 17 and 18 would have been obvious to the artisan in light of the disclosures of storing error values and storing correct flip flop values for comparison purposes in Missios. The discussion with respect to figures subsequent to Fig. 1 in Missios indicate that a particular failing component may be identified. Whether the final storage media is volatile or nonvolatile as recited in dependent claim 18, we consider that the artisan would have found it obvious to have utilized either in which to store any defect or error information discovered during the testing operation.

We reverse the rejection of dependent claim 19 essentially for the same reason as we reversed the rejection of the features recited in dependent claim 2. Because claim 20 depends from claim 19, we also reverse the rejection of this claim.

In view of the above discussion, we do not agree with the examiner's interpretation of the reference indicating a view that Missios does not explicitly teach the retrying of an instruction or the retrying of an instruction at a reduced

clock frequency. The examiner's reasoning also appears to overuse the assertion that features were well known in the prior art without providing appropriate prior art to add evidence to that assertion.

It is also apparent that to the extent we affirm the rejection as noted earlier, we also do not agree with all of appellants' assertions in the brief and reply brief. We do not construe the independent claims on appeal as asserting positively a feature requiring fault tolerance and error recovery to the extent argued. Nor does the initial retry operation of claims 1, 5 and 15 reciting this feature specifically require it to be at a normal clock frequency. It is further noted, however, that an initial normal clock frequency test is a part of block D1 in Fig. 1 of Missios and at least a portion of each of blocks D3, D6 and D9 as explained beginning at col. 2.

Additionally, to the extent recited in the independent claims on appeal, and in contradistinction to the assertions made, there is no clear recitation of the requirement of a stream of instructions in each independent claim but in some cases merely an "operation" associated with the operation of

the overall system or an operation associated with "at least one" of an instruction, which features are clearly taught or clearly inferred from an artisan's perspective from the identified teachings and showings in Missios. We therefore do not agree with appellants' assertions that the reference teaches away from the features recited as identified by us in our earlier discussion.

To the extent Missios clearly teaches a testing procedure to determine which of a plurality of clock periods and error is occurring for specific identification purposes, it clearly would have been obvious to the artisan to have performed similar operations with respect to actual instruction sequences to determine which of a plurality of instructions caused a given error or operation associated therewith. Such a check point retry operation known in the prior art as identified at page 2 of appellants' specification discussing the prior art is analogous to the features of Missios. Furthermore, it goes without saying that the feature of retrying operations in the claims that recite such a feature is clearly analogous to the repeating operations associated with the network in Missios. Indeed, the known self-test

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mechanisms described by appellants in the admitted prior art in the paragraph bridging pages 1 and 2 of the specification as filed clearly is closely aligned with the teachings in Missios as they relate to testing at a first or normal clock speed followed by a subsequent lower clock speed to determine the specific nature of the defects causing the error.

Finally, the related appeal identified earlier in footnote 2 in this opinion relates to an appeal stemming from an application which is a continuation of this application. That application in the related appeal appears to have been voluntarily filed. The appeal in that application is later filed than this one, and because the claims in that appeal relate to variations of the subject matter claimed in this appeal, we hereby remand this application for the examiner to consider on the record the issue of obviousness-type double patenting in any further proceedings as to this application as it relates to the other application.

To recap, we have sustained the rejection of claims 1, 5, 6, 11 to 13, 15, 17 and 18 and have reversed the rejection of the remaining claims, namely claims 2 through 4, 7 through 10, 14,

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16, 19 and 20. Since our reasoning relies to some extent upon appellants' admitted prior art as well as new insights not set forth by the examiner before as to the teachings in Missios, we hereby designate the affirmance of the above-noted claims as a new ground of rejection within 37 CFR § 1.196(b).

In addition to affirming the examiner's rejection of one or more claims, this decision contains a new ground of rejection pursuant to 37 CFR § 1.196(b) (amended effective Dec. 1, 1997, by final rule notice, 62 Fed. Reg. 53,131, 53,197 (Oct. 10, 1997), 1203 Off. Gaz. Pat. & Trademark Office 63, 122 (Oct. 21, 1997)). 37 CFR § 1.196(b) provides, "A new ground of rejection shall not be considered final for purposes of judicial review."

Regarding any affirmed rejection, 37 CFR § 1.197(b) provides:

(b) Appellant may file a single request for rehearing within two months from the date of the original decision . . . .

37 CFR § 1.196(b) also provides that the appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new

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ground of rejection to avoid termination of proceedings (37  
CFR § 1.197(c)) as to the rejected claims:

(1) Submit an appropriate amendment of the claims so rejected or a showing of facts relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the application will be remanded to the examiner. . . .

(2) Request that the application be reheard under § 1.197(b) by the Board of Patent Appeals and Interferences upon the same record. . . .

Should the appellants elect to prosecute further before the Primary Examiner pursuant to 37 CFR § 1.196(b)(1), in order to preserve the right to seek review under 35 U.S.C. §§ 141 or 145 with respect to the affirmed rejection, the effective date of the affirmance is deferred until conclusion of the prosecution before the examiner unless, as a mere incident to the limited prosecution, the affirmed rejection is overcome.

If the appellants elect prosecution before the examiner and this does not result in allowance of the application, abandonment or a second appeal, this case should be returned to the Board of Patent Appeals and Interferences for final action on the affirmed rejection, including any timely request for rehearing thereof.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART; 37 CFR § 1.196(b); and REMANDED

JAMES D. THOMAS  
Administrative Patent Judge

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